Circuits

by

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Chapter 1
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Figure 1-2: Cell-phone block diagram. Each block consists of multiple circuits that together provide the required functionality.

Figure 1-3: The functionality of a circuit is discerned by applying the tools of circuit analysis. The reverse process, namely the realization of a circuit whose functionality meets a set of specifications, is called circuit synthesis or design.

Figure 1-4: (a) Block diagram, (b) circuit diagram, (c) printed-circuit-board (PCB) layout, (d) photograph of a touch-sensor circuit.

Figure 1-5: Diagram representing a circuit that contains dc and ac sources, passive elements (six resistors, one capacitor, and one inductor), and one active element (operational amplifier). Ordinary nodes are in yellow, extraordinary nodes in other colors, and the ground node in black.

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Figure 1-9: The current flowing in the wire is due to electron transport through a drift process, as illustrated by the magnified structure of the wire.

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Figure 1-17: Ground is any point in the circuit selected to serve as a reference point for all points in the circuit.

Figure 1-18: An ideal voltmeter measures the voltage difference between two points (such as nodes 1 and 2 in (a)) without interfering with the circuit (i.e., no current runs through the voltmeter). Similarly, an ideal ammeter measures the current magnitude and direction with no voltage drop across itself. In (b), one voltmeter is used to measure voltage difference V_{ab} and another to measure node voltage V_a. Note the polarity of the meters. The red leads are connected to the $+$ terminals of the voltages or currents, and the black leads are connected to the $-$ terminals of the voltages or currents. For the voltmeter, the red port on the left is $(+)$ and the black port in the center is $(-)$, and for the ammeter the red port on the right is the $(+)$.

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$$\frac{v_2}{v_1} = \frac{N_2}{N_1} = n, \qquad \frac{i_2}{i_1} = \frac{N_1}{N_2} = \frac{1}{n}, \qquad \frac{p_2}{p_1} = \frac{v_2 i_2}{v_1 i_1} = 1 \quad .$$

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Figure 9-33: AC analysis plots for the circuit in **Fig.** 9.31 generated with the Parameter Sweep tool in Example 9-14. The capacitance was varied from 1 to 10 pF.

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Figure 10-5: The three-phase source and load circuits can be connected in four possible arrangements: Y-Y, Y-Δ, Δ-Y, and Δ-Δ. In each arrangement, the source and load circuits are connected via transmission lines carrying ***line currents*** $\mathbf{I}_{\mathrm{L}_1}$, $\mathbf{I}_{\mathrm{L}_2}$, and $\mathbf{I}_{\mathrm{L}_3}$. [Parts (c) and (d) follow on the next page.]

Figure 10-5(continued): (**Fig. 10-5** continued)

Figure 10-6: Three-phase Y source connected to a Y load circuit via transmission lines.

Figure 10-7: Y-Δ transformation for balanced load circuits.

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Chapter 12
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Chapter 13
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Figure 13-22: Complete Multisim circuit of the ΣΔ modulator.

Figure 13-23: A 1 Hz sinusoidal ac signal, $\upsilon_{in}(t)$, blue trace, is converted to a series of pulses at the output, $\upsilon_{out}(t)$, red trace, by the Sigma Delta modulator. Note that the duration of the pulses is related to the instantaneous level of voltage $\upsilon_{in}(t)$.

Figure 1.1 Cell phone.

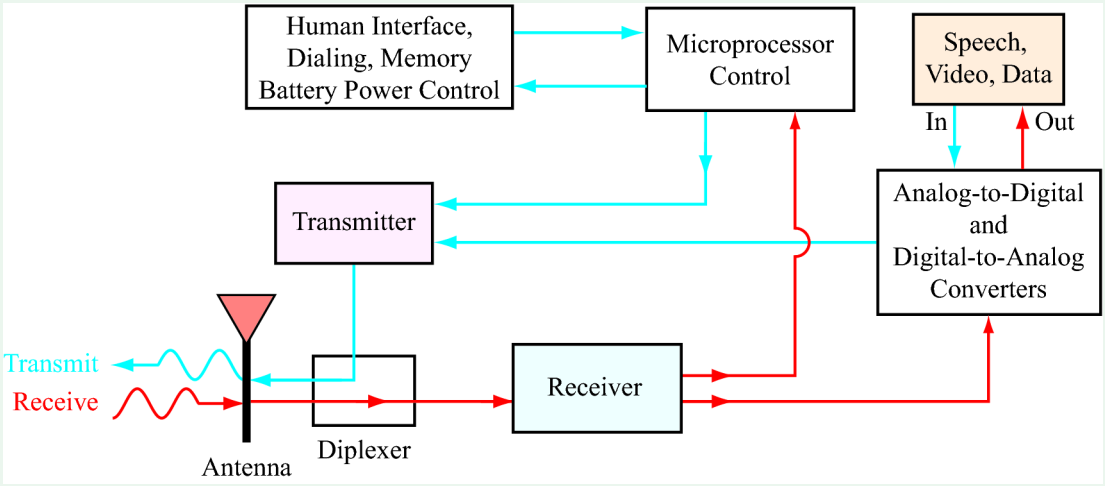


Figure 1.2 Basic cell-phone block diagram. Each block consists of multiple circuits that together provide the required functionality.

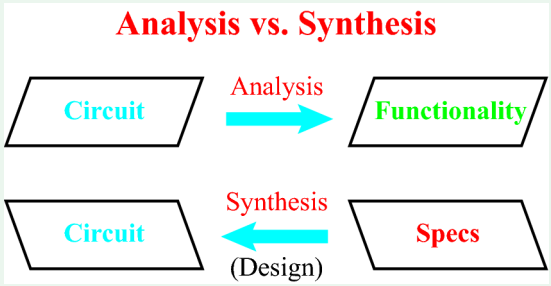
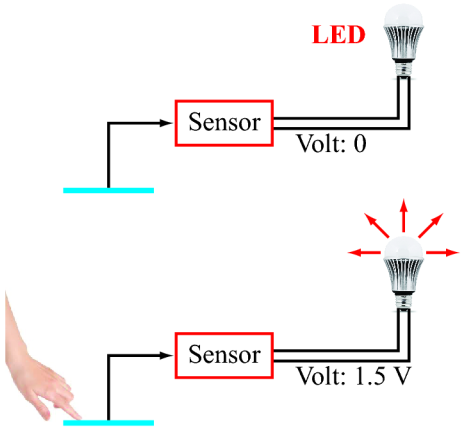
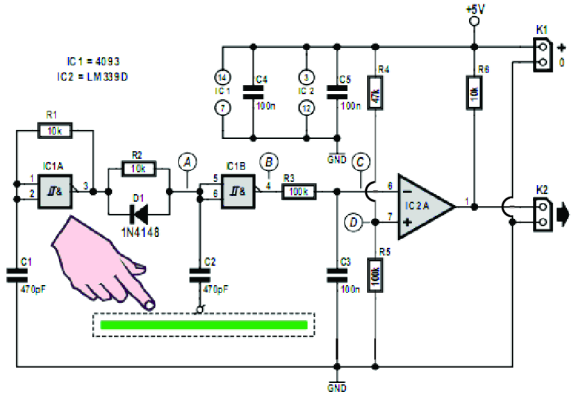


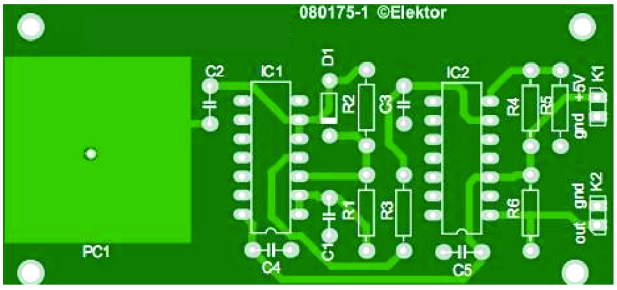
Figure 1.3 The functionality of a circuit is discerned by applying the tools of circuit analysis. The reverse process, namely the realization of a circuit whose functionality meets a set of specifications, is called circuit synthesis or design.



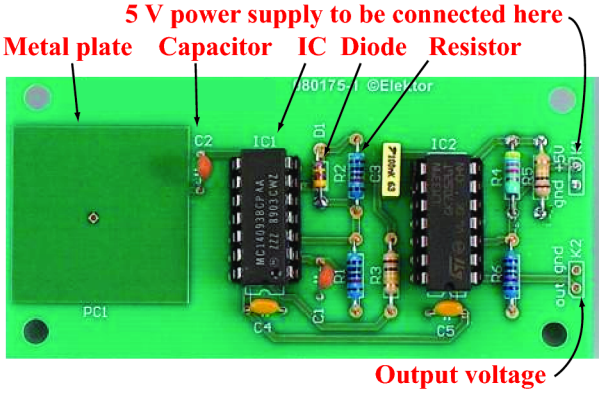
(a) Block diagram



(b) Circuit diagram



(c) Printed circuit board (PCB)



(d) Actual circuit

Figure 1.4 (a) Block diagram, (b) circuit diagram, (c) printed-circuit-board (PCB) layout, (d) photograph of a touch-sensor circuit.

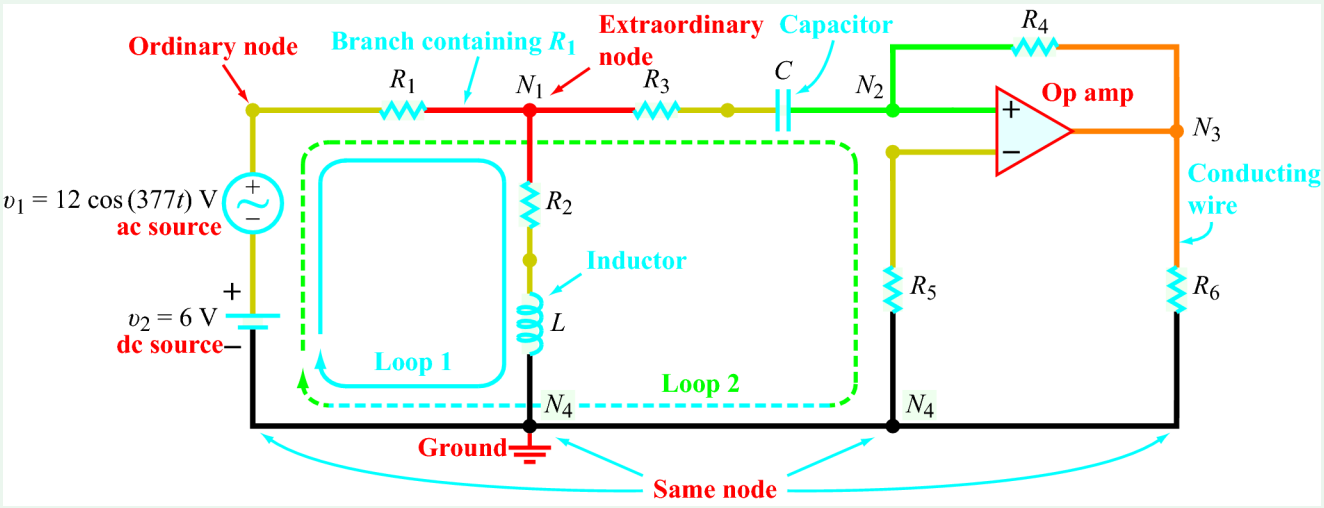


Figure 1.5 Diagram representing a circuit that contains dc and ac sources, passive elements (six resistors, one capacitor, and one inductor), and one active element (operational amplifier). Ordinary nodes are in yellow, extraordinary nodes in other colors, and the ground node in black.

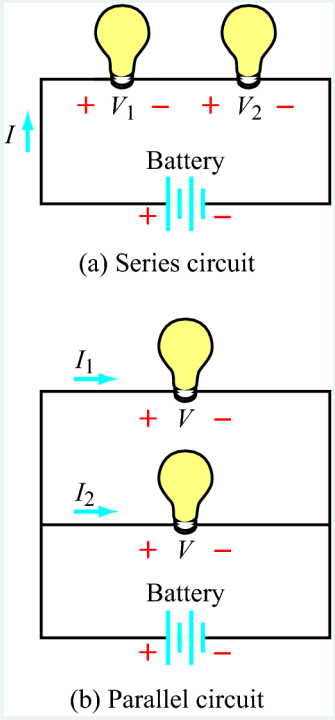


Figure 1.6 Two light bulbs connected (a) in series and (b) in parallel.

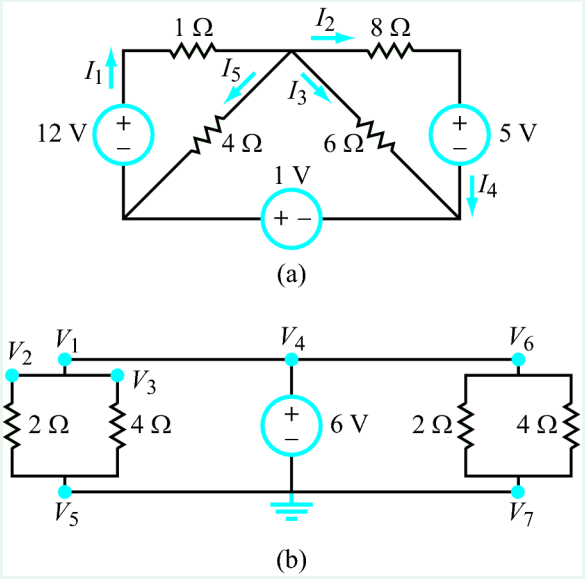


Figure 1.7 Circuits for Example 1-1.

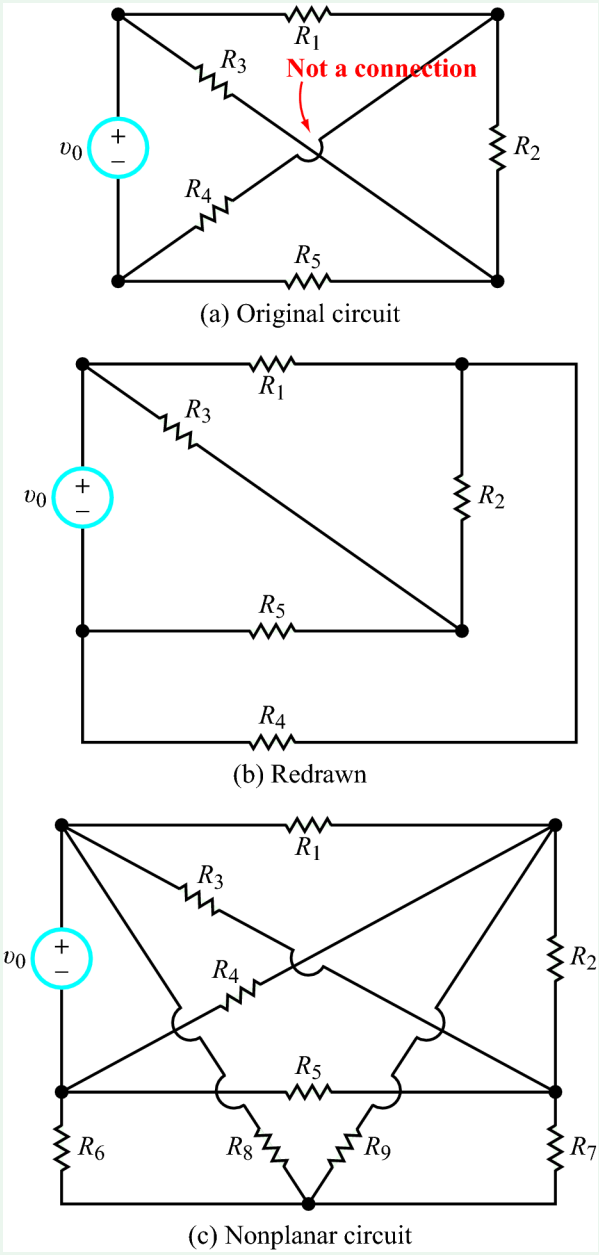


Figure 1.8 The branches containing R_3 and R_4 in (a) *appear to cross* over one another, but redrawing the circuit as in (b) avoids the crossover, thereby demonstrating that the circuit is planar.

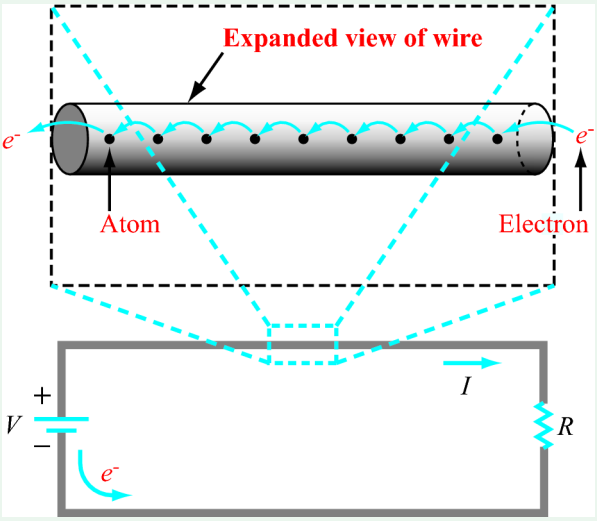


Figure 1.9 The current flowing in the wire is due to electron transport through a drift process, as illustrated by the magnified structure of the wire.

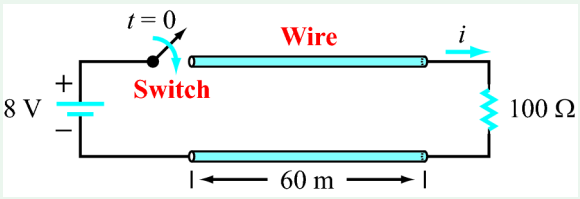


Figure 1.10 After closing the switch, it takes only 0.2 μs to observe a current in the resistor.

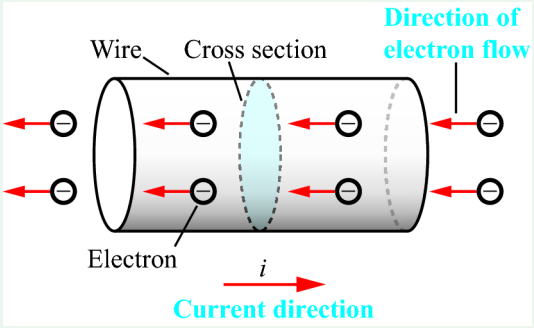


Figure 1.11 Direction of (positive) current flow through a conductor is opposite that of electrons.

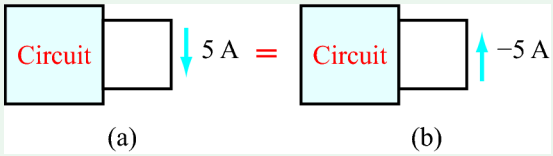


Figure 1.12 A current of 5 A flowing "downward" is the same as −5 A flowing "upward" through the wire.

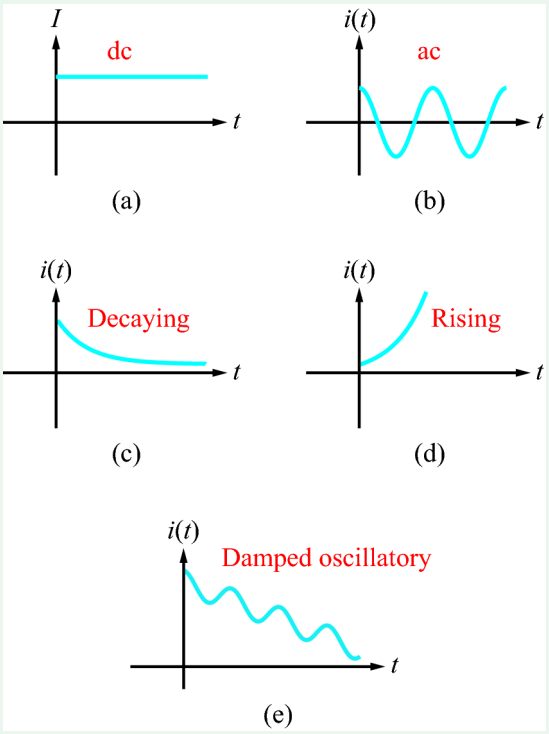


Figure 1.13 Graphical illustrations of various types of current variations with time.

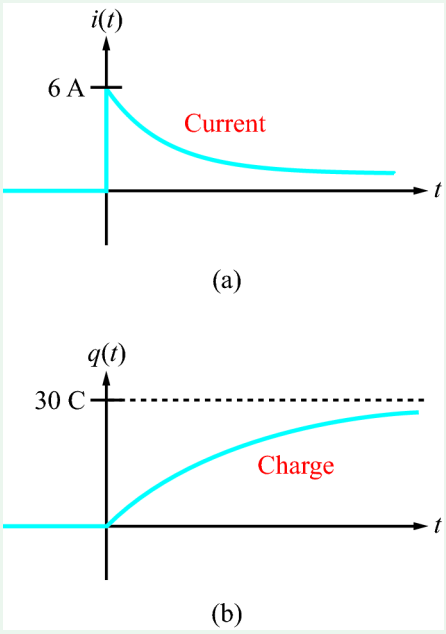
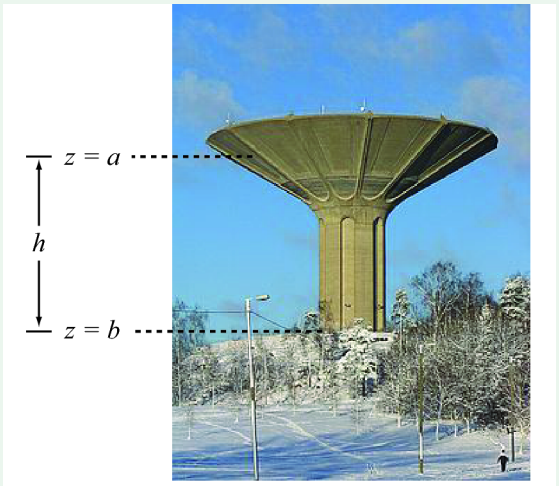
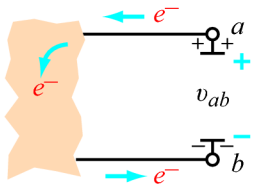


Figure 1.14 The current $i(t)$ displayed in (a) generates the cumulative charge $q(t)$ displayed in (b).



(a) Raising water from ground level at b to height a



(b) Moving charge from a to b

Figure 1.15 Moving charge dq through the material in (b) is analogous to raising mass dm in (a).

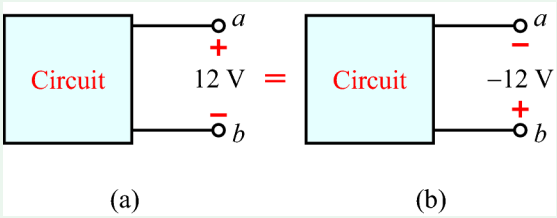


Figure 1.16 In (a), with the (+) designation at node a, $V_{ab} = 12$ V. In (b), with the (+) designation at node b, $V_{ba} = -12$ V, which is equivalent to $V_{ab} = 12$ V. [That is, $V_{ab} = -V_{ba}$.]

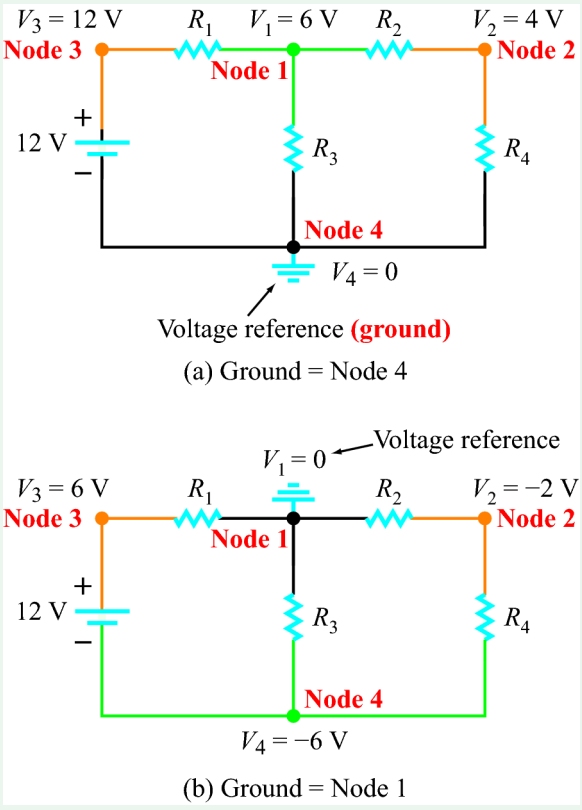
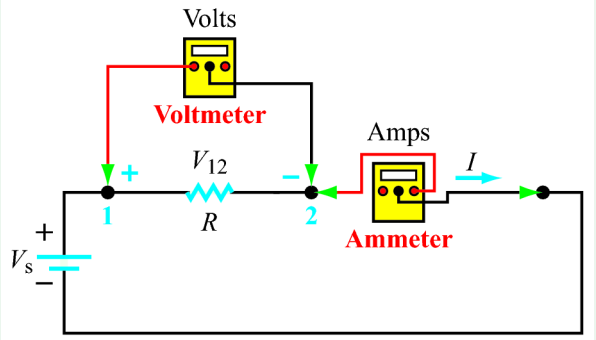
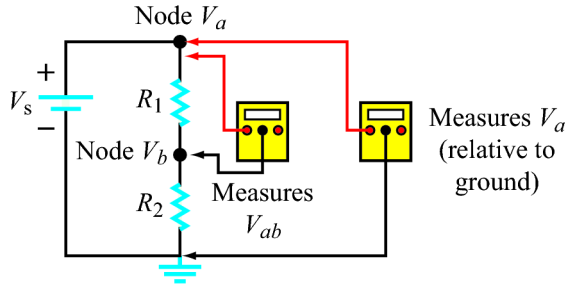


Figure 1.17 Ground is any point in the circuit selected to serve as a reference point for all points in the circuit.



(a) Voltmeter and ammeter connections



(b) Voltmeters connected to measure voltage difference V_{ab} and node voltage V_a (relative to ground)

Figure 1.18 An ideal voltmeter measures the voltage difference between two points (such as nodes 1 and 2 in (a)) without interfering with the circuit (i.e., no current runs through the voltmeter). Similarly, an ideal ammeter measures the current magnitude and direction with no voltage drop across itself. In (b), one voltmeter is used to measure voltage difference V_{ab} and another to measure node voltage V_a. Note the polarity of the meters. The red leads are connected to the $+$ terminals of the voltages or currents, and the black leads are connected to the $-$ terminals of the voltages or currents. For the voltmeter, the red port on the left is $(+)$ and the black port in the center is $(-)$, and for the ammeter the red port on the right is the $(+)$.

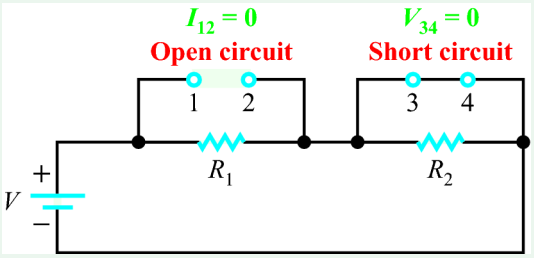


Figure 1.19 Open circuit between terminals 1 and 2, and short circuit between terminals 3 and 4.

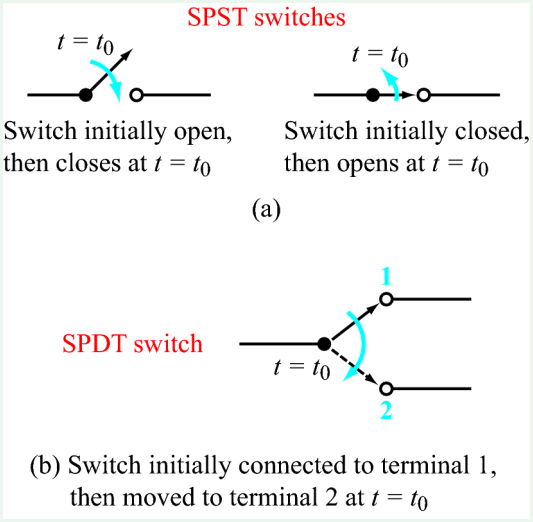


Figure 1.20 (a) Single-pole single-throw (SPST) and (b) single-pole double-throw (SPDT) switches.

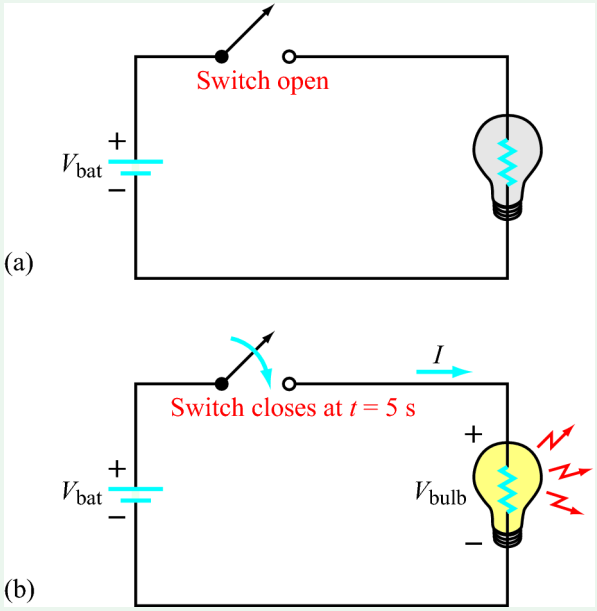


Figure 1.21 Current flow through a resistor (light-bulb filament) after closing the witch.

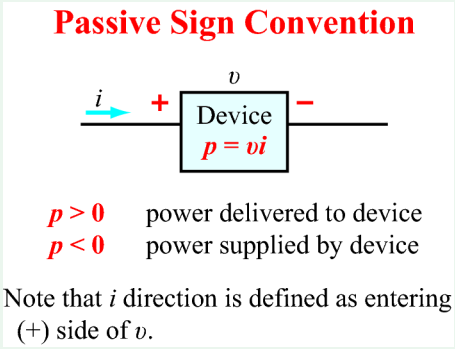


Figure 1.22 Passive sign convention.

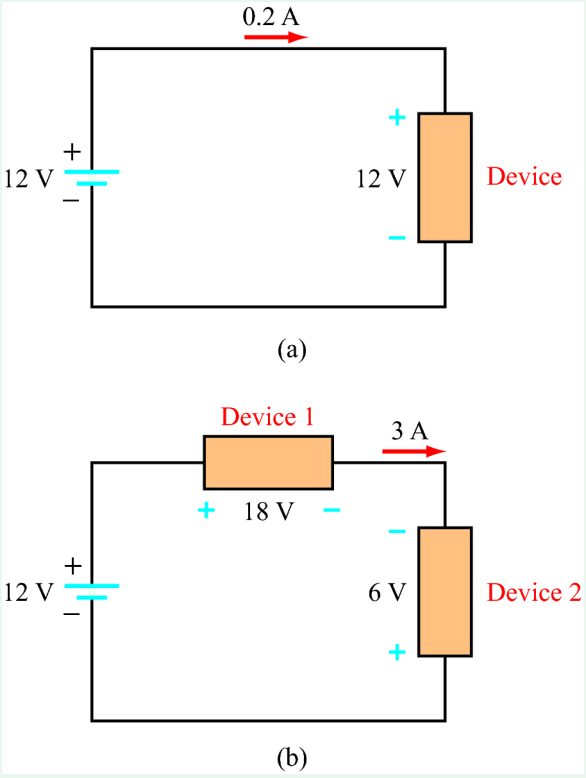


Figure 1.23 Circuits for Example 1-5.

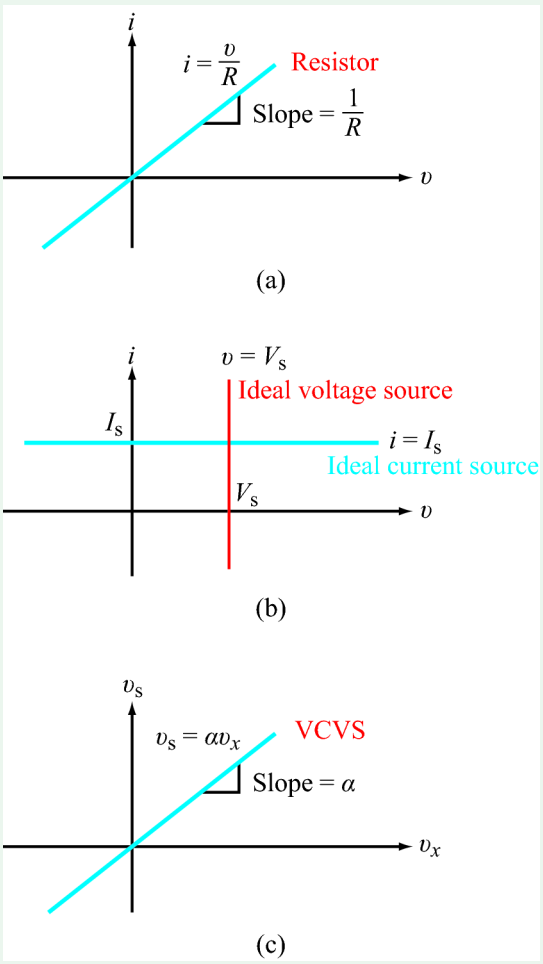
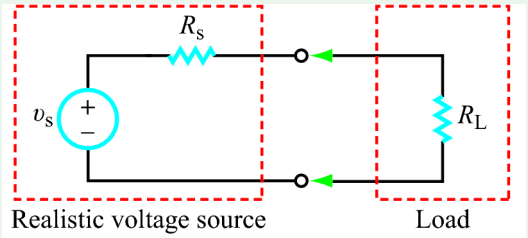
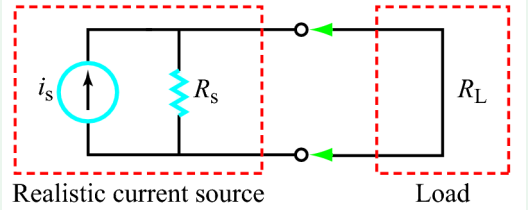


Figure 1.24 i–v relationships for (a) an ideal resistor, (b) ideal, independent current and voltage sources, and (c) a dependent, voltage-controlled voltage source (VCVS).



(a) Realistic voltage source connected to load R_L



(b) Realistic current source connected to load R_L

Figure 1.25 (a) A realistic voltage source has a nonzero series resistance R_s, which can be replaced with a short circuit if R_s is much smaller than the load resistance R_L. (b) A realistic current source has a nonzero parallel resistance R_s, which can be replaced with an open circuit if $R_s \gg R_L$.

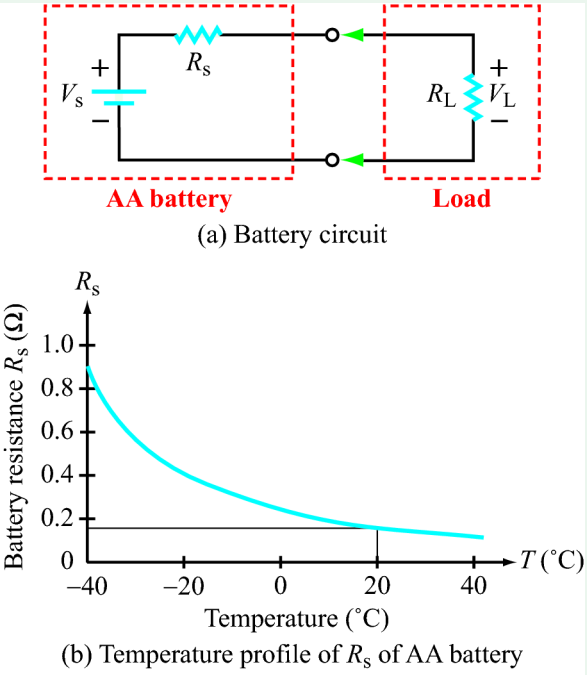


Figure 1.26 Circuit and temperature profile of battery's R_S of Example 1-7.

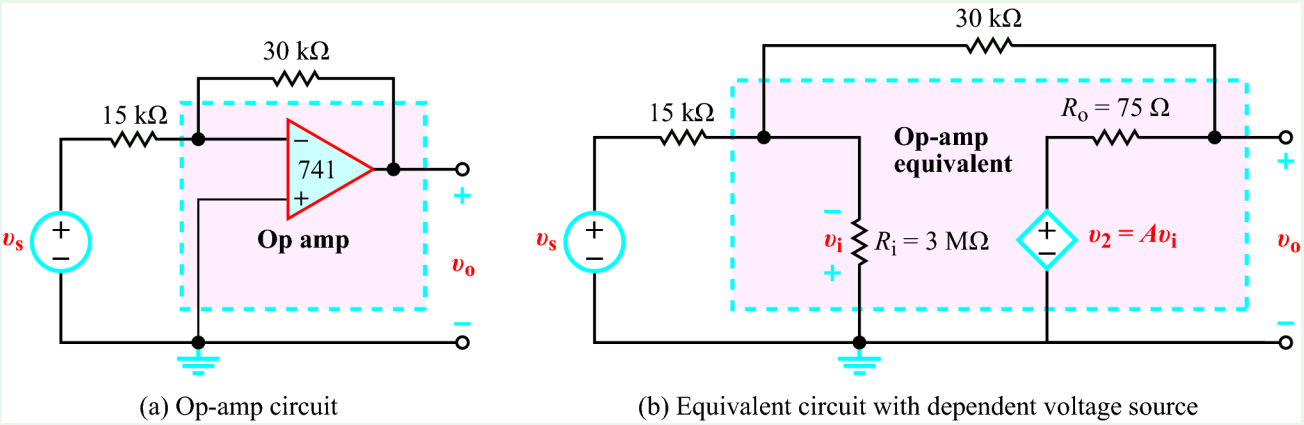


Figure 1.27 An operational amplifier is a complex device, but its circuit behavior can be represented in terms of a simple equivalent circuit that includes a dependent voltage source.

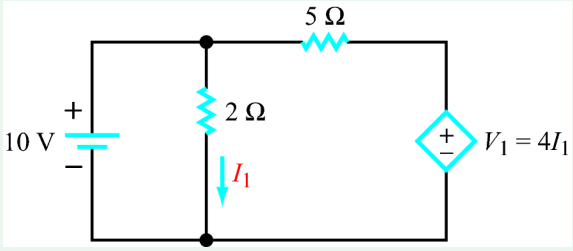


Figure 1.28 Circuit for Example 1-7.

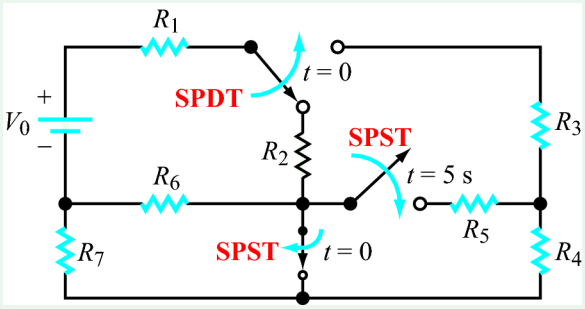
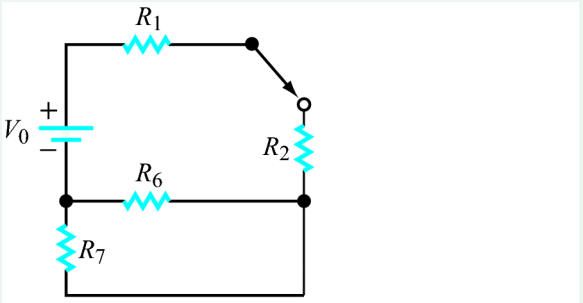
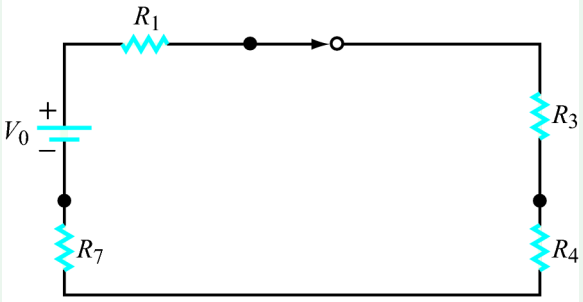


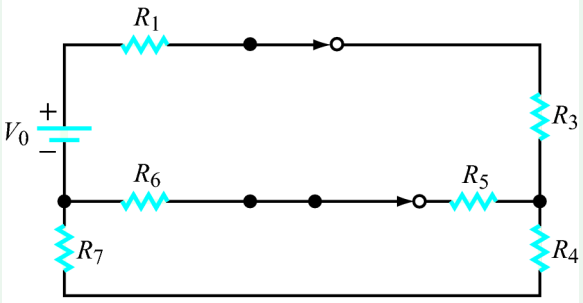
Figure 1.29 Circuit for Example 1-9.



(a) $t < 0$



(b) $0 \leq t < 5$ s



(c) $t \geq 5$ s

Figure 1.30 Solutions for circuit in **Fig.** 1.29.

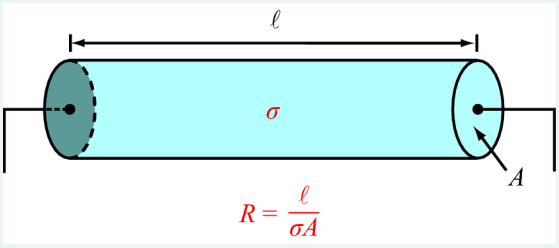


Figure 2.1 Longitudinal resistor of conductivity σ, length ℓ, and cross-sectional area A.

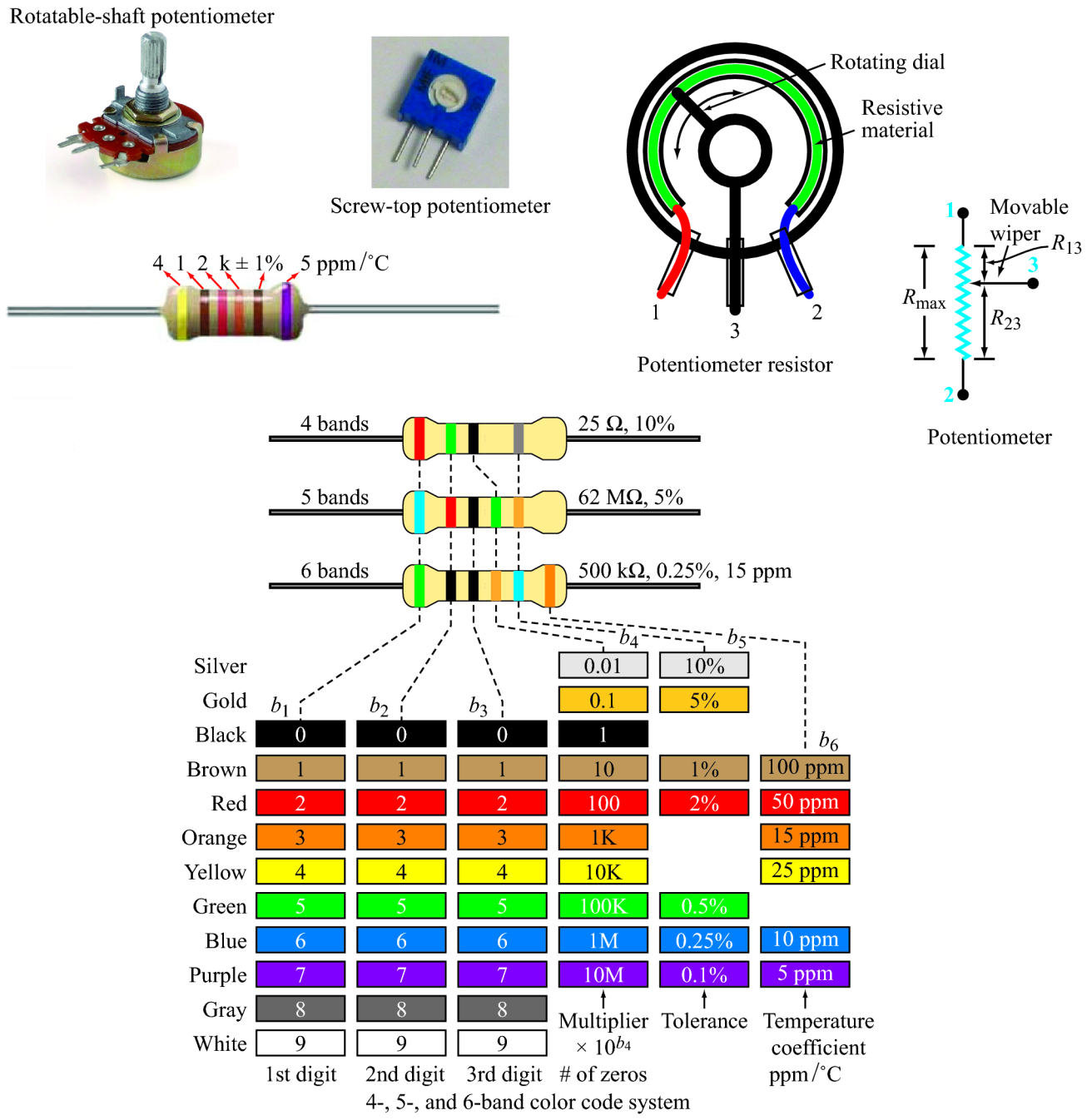


Figure 2.2 Various types of resistors. Tubular-shaped resistors usually are color-coded by 4-, 5-, or 6-band systems.

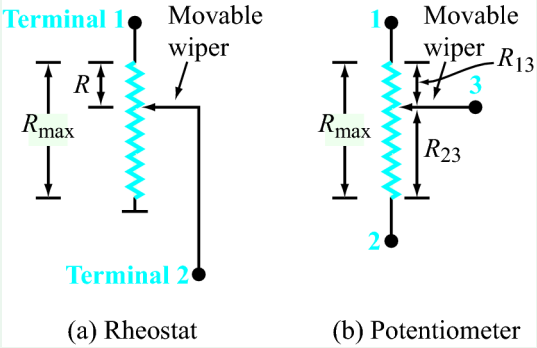


Figure 2.3 (a) A rheostat is used to set the resistance between terminals 1 and 2 at any value between zero and R_{max}; (b) the wiper in a potentiometer divides the resistance R_{max} among R_{13} and R_{23}.

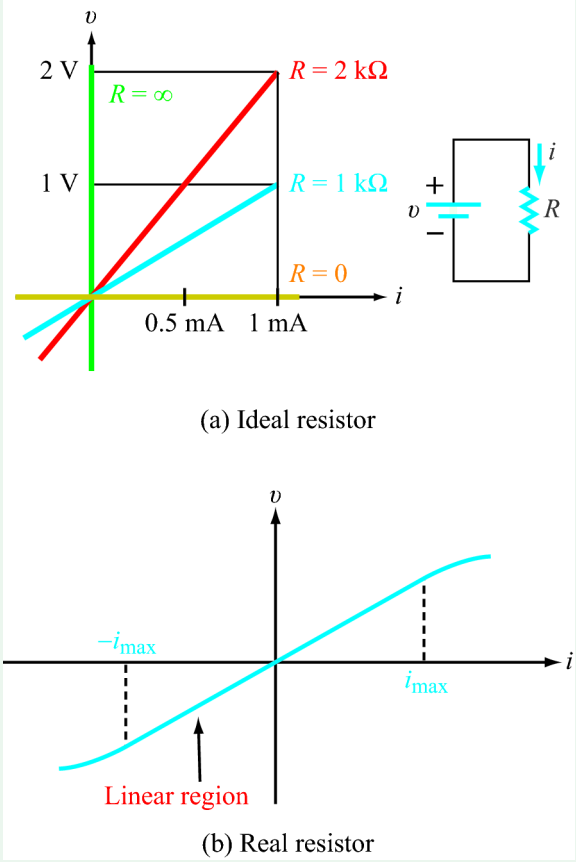


Figure 2.4 i–v responses of ideal and real resistors.

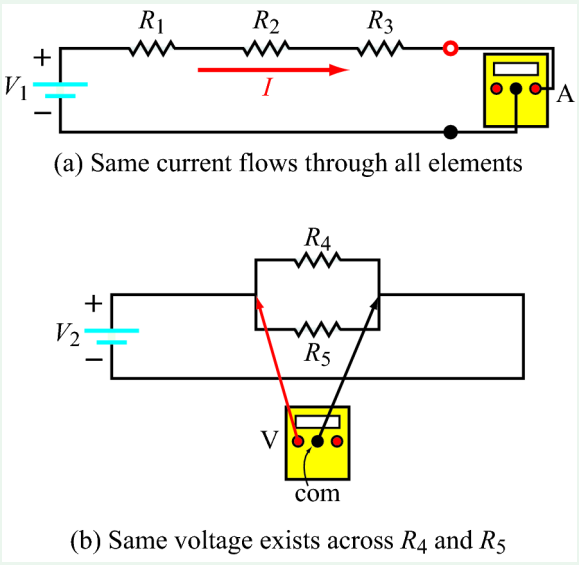


Figure 2.5 In-series and in-parallel connections.

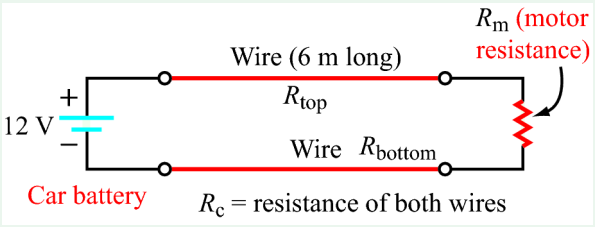


Figure 2.6 Circuit for Example 2-1.

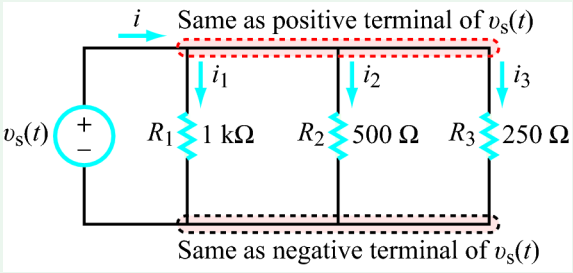


Figure 2.7 Circuit for Example 2-2.

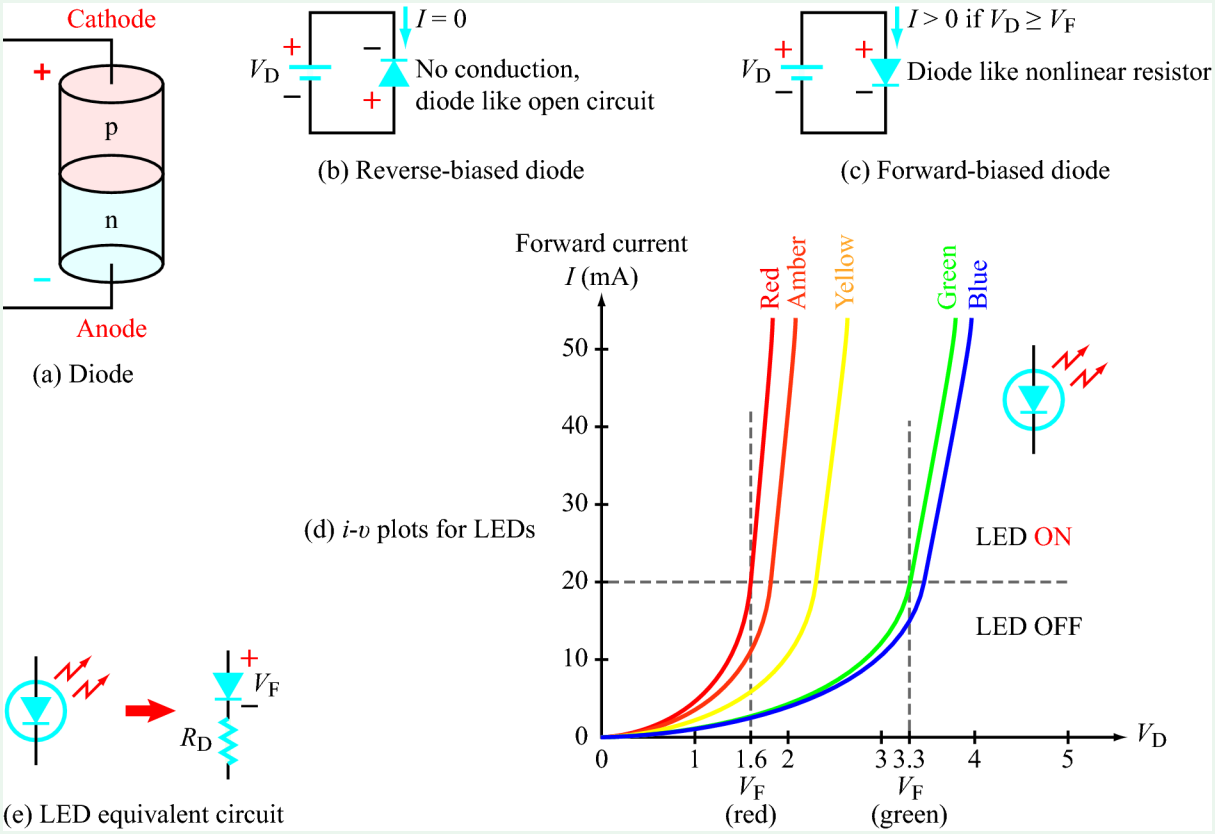


Figure 2.8 p-n junction diode (a) configuration, (b) reverse biased, (c) forward biased, (d) typical i-υ plots for LEDs, and (e) LED equivalent circuit.

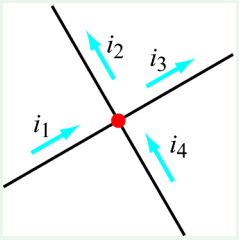


Figure 2.9 Currents at a node.

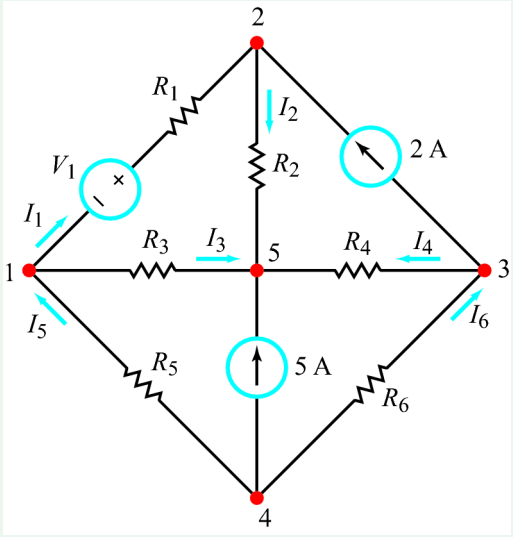


Figure 2.10 Circuit for Example 2-3.

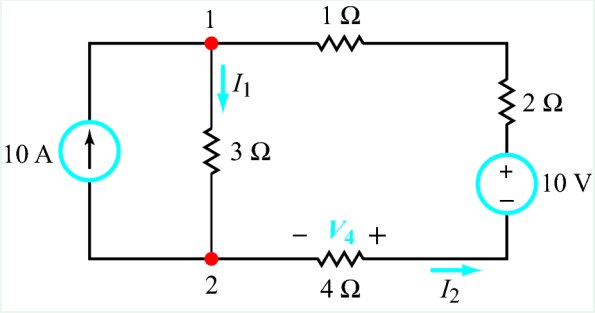


Figure 2.11 Circuit for Example 2-4.

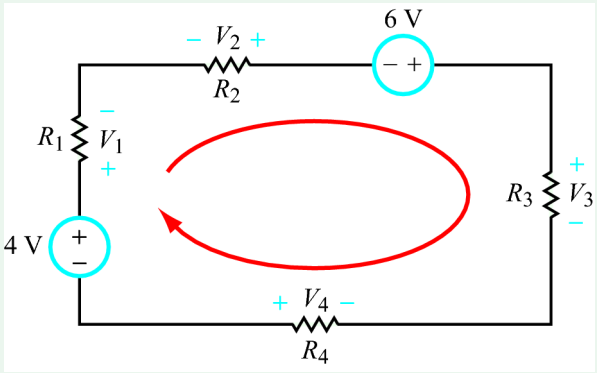


Figure 2.12 One-loop circuit.

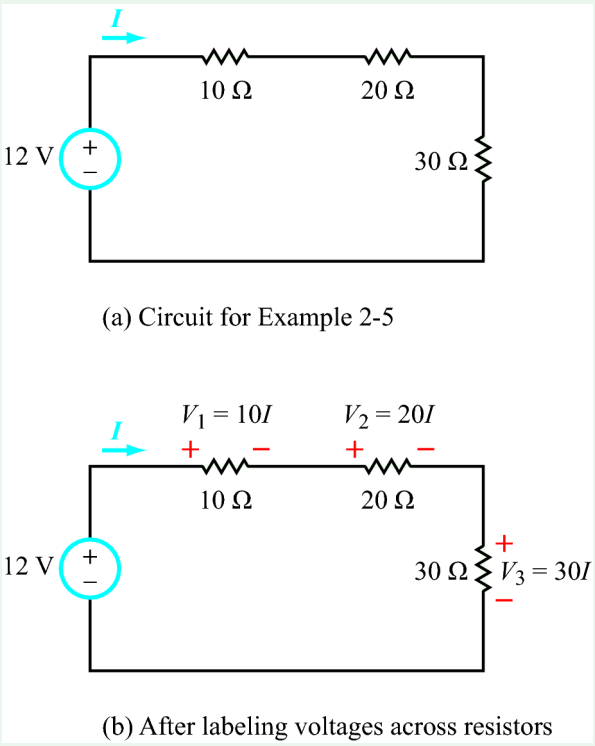


Figure 2.13 Circuit for Example 2-5 before and after labeling voltages across the three resistors with polarities consistent with Ohm's law.

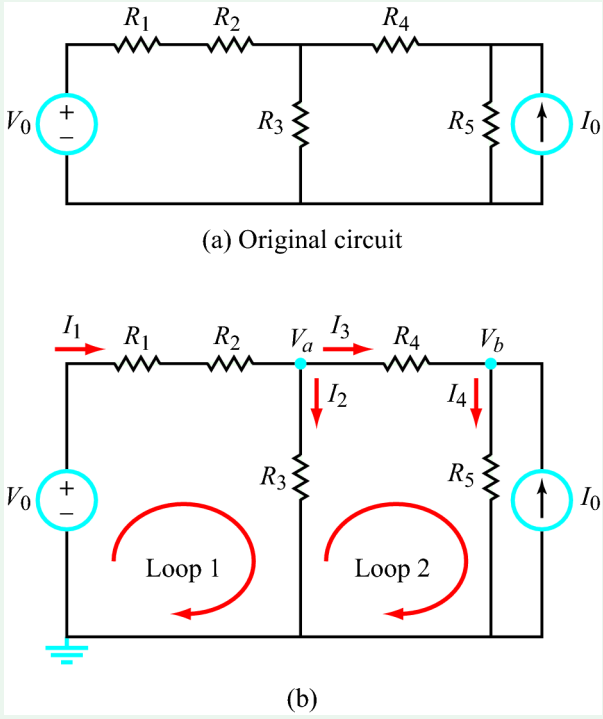
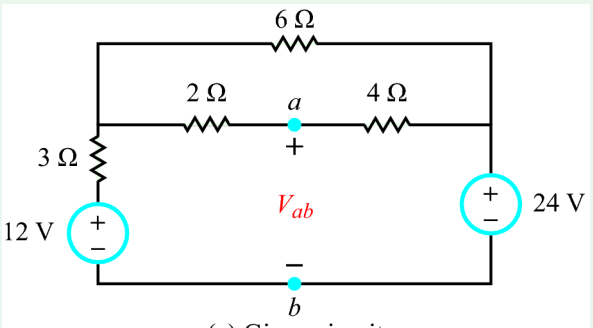
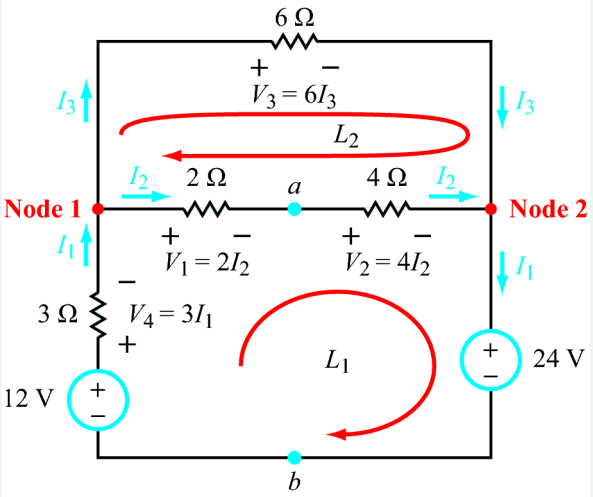


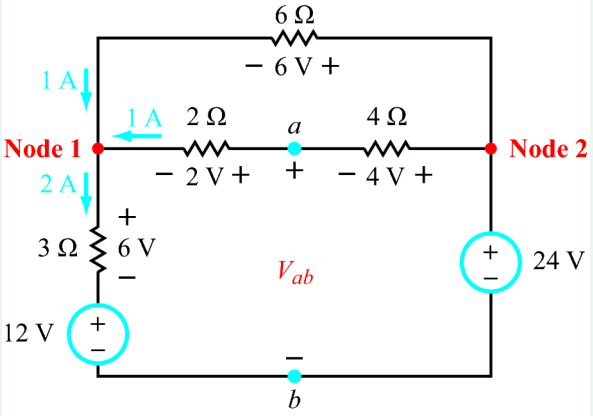
Figure 2.14 Circuit for Example 2-6.



(a) Given circuit

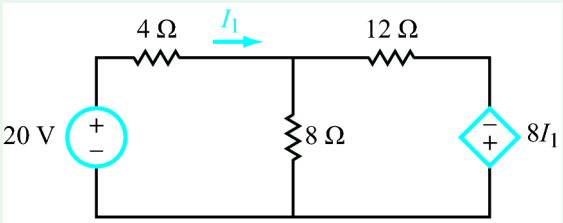


(b) After assigning currents at nodes 1 and 2

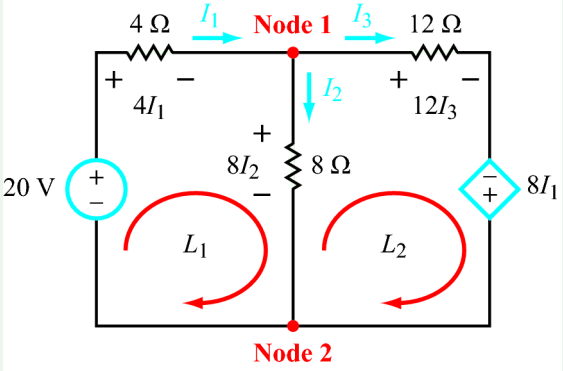


(c) After completing solution

Figure 2.15 Circuit for Example 2-7.



(a) Given circuit



(b) After assigning currents at node 1

Figure 2.16 Circuit for Example 2-8.

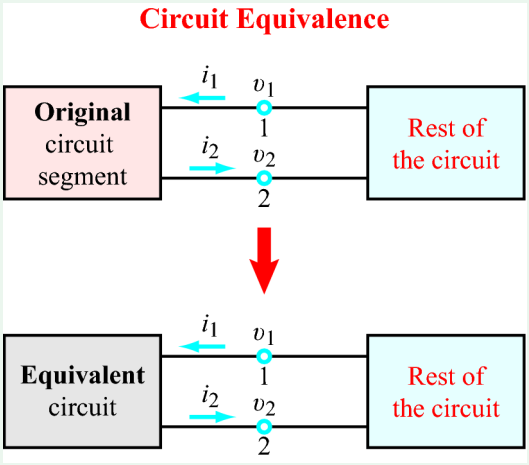
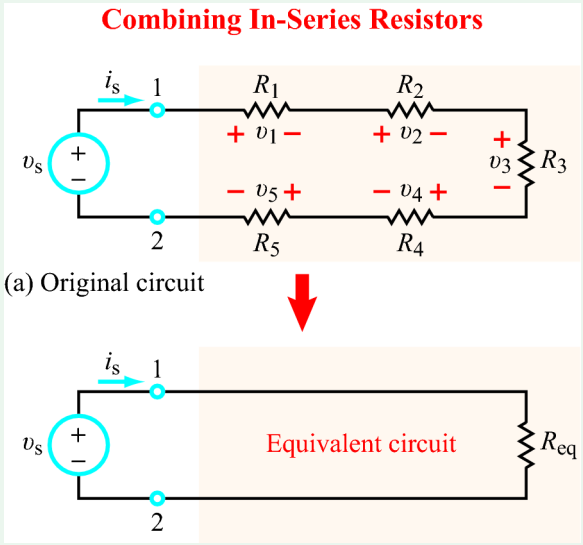
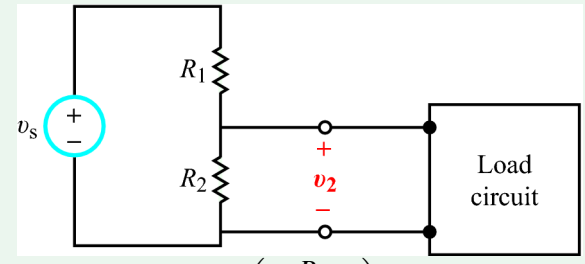


Figure 2.17 Circuit equivalence requires that the equivalent circuit exhibit the same i–υ characteristic as the original circuit.

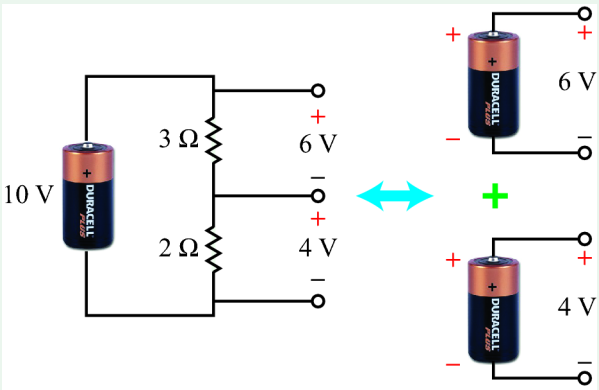


(b) $R_{eq} = R_1 + R_2 + R_3 + R_4 + R_5$

Figure 2.18 In a single-loop circuit, R_{eq} is equal to the sum of the resistors.



(a) $$v_2 = \left(\frac{R_2}{R_1 + R_2}\right) v_s$$



(b) Voltage divider is equivalent to subdividing a battery into two separate batteries

Figure 2.19 Voltage dividers are important tools in circuit analysis and design.

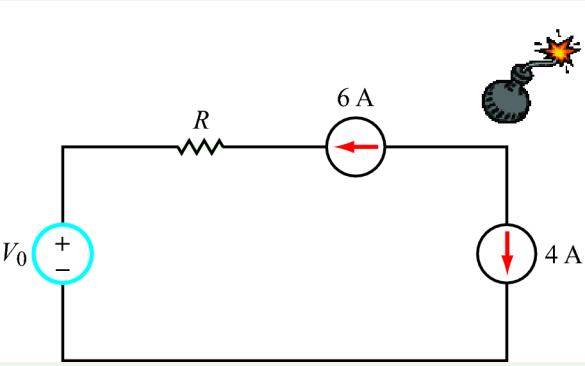
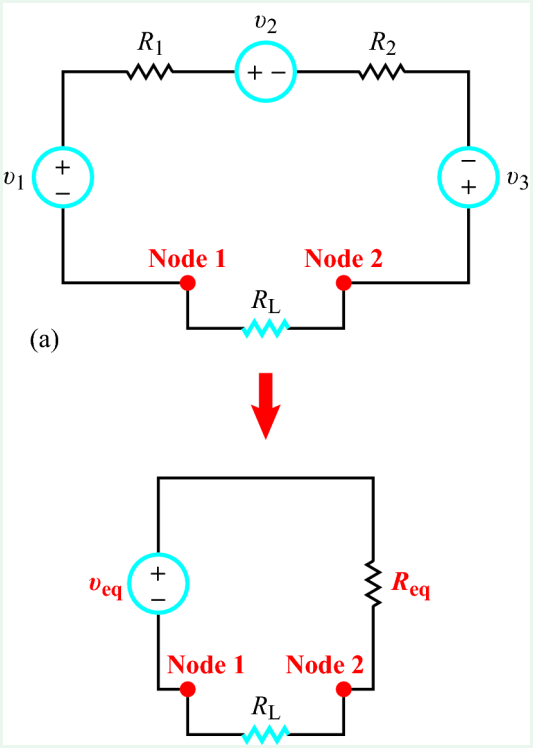
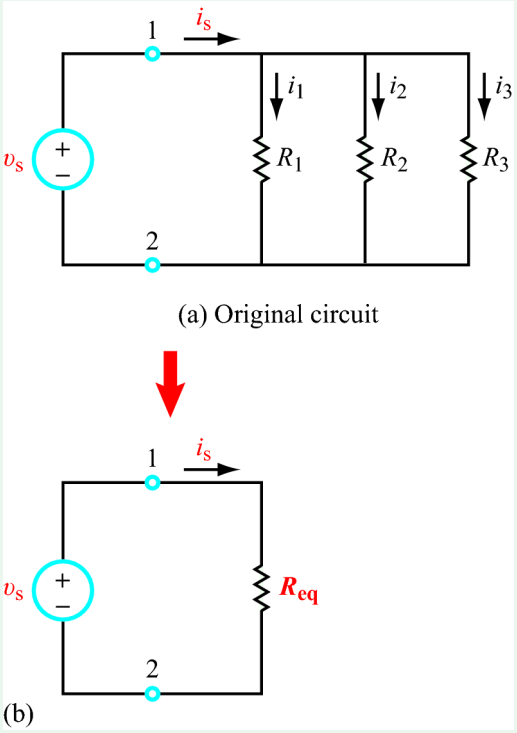


Figure 2.20 Unrealizable circuit; two current sources with different magnitudes or directions cannot be connected in series.



(b) $v_{eq} = v_1 - v_2 + v_3 \qquad R_{eq} = R_1 + R_2$

Figure 2.21 In-series voltage sources can be added together algebraically.



$$R_{eq} = \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)^{-1} \qquad i_2 = \left(\frac{R_{eq}}{R_2}\right) i_s$$

Figure 2.22 Voltage source connected to a parallel combination of three resistors.

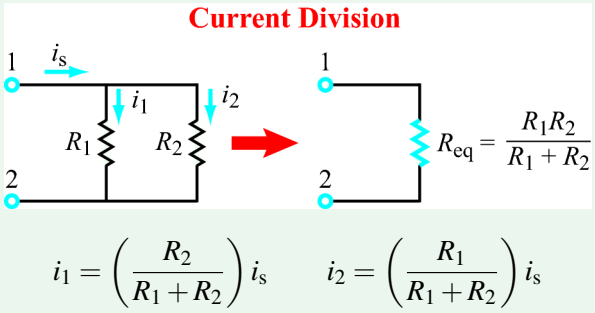


Figure 2.23 Equivalent circuit for two resistors in parallel.

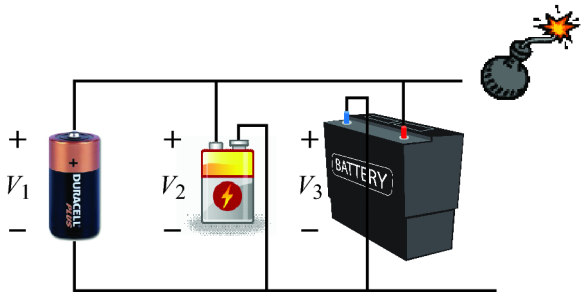
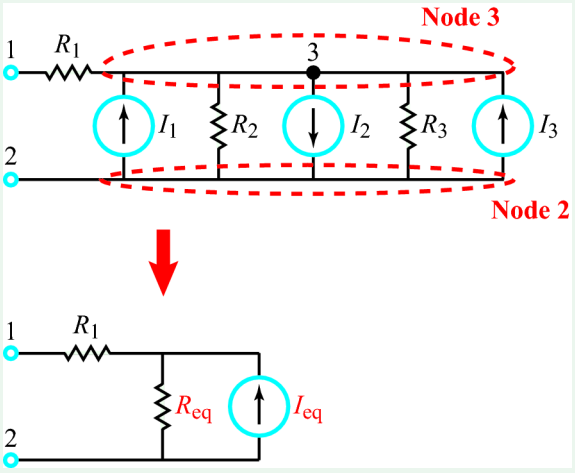


Figure 2.24 This is an unrealizable circuit unless all voltage sources have identical voltages and polarities; that is, $V_1 = V_2 = V_3$.



$$R_{eq} = R_2 \parallel R_3 = \frac{R_2 R_3}{R_2 + R_3} \qquad I_{eq} = I_1 - I_2 + I_3$$

Figure 2.25 Adding current sources connected in parallel.

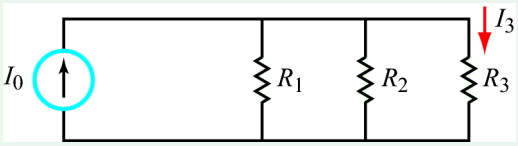


Figure 2.26 Circuit for Example 2-10.

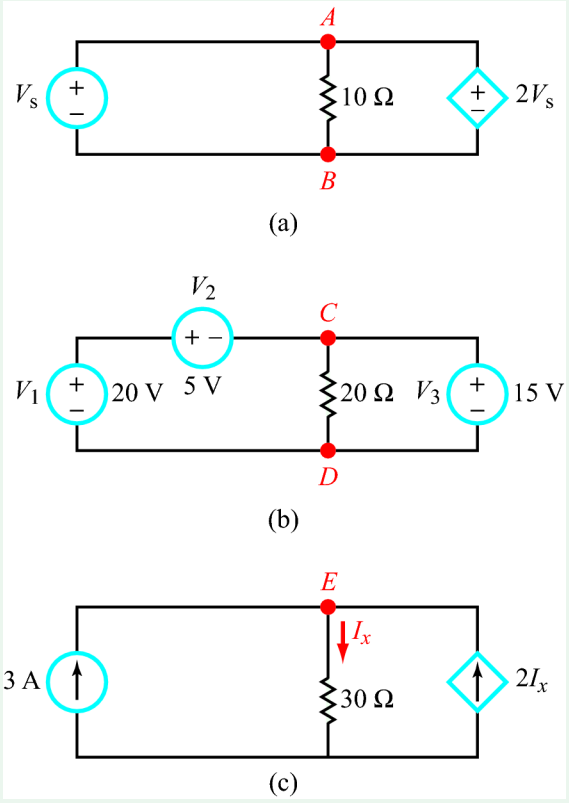


Figure 2.27 Circuits of Example 2-11.

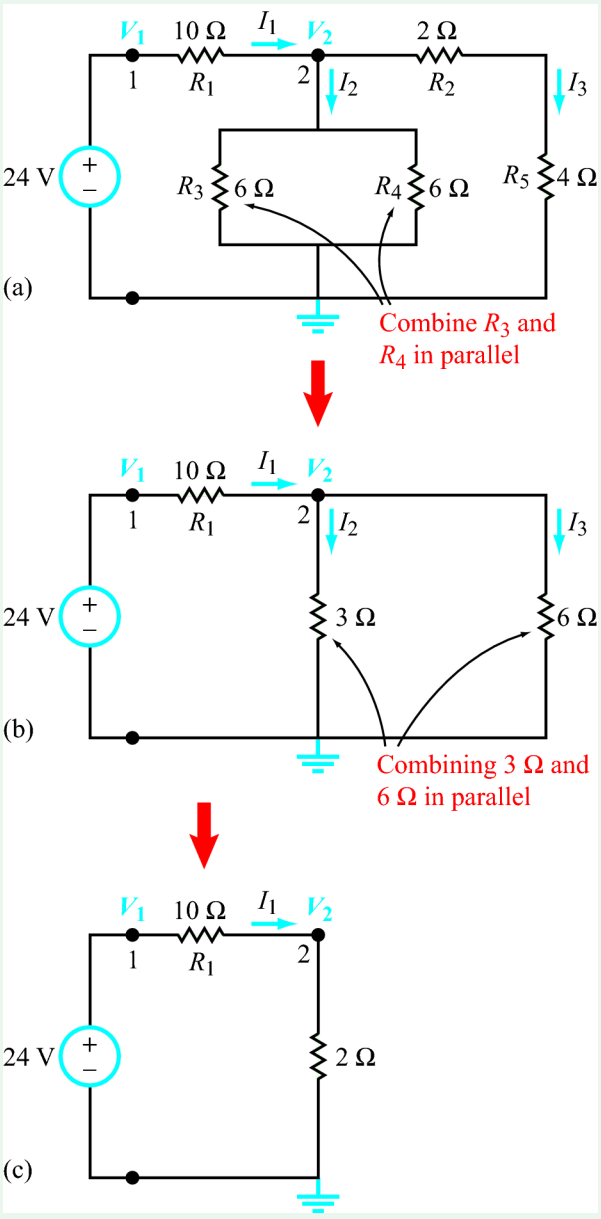


Figure 2.28 Example 2-12. (a) Original circuit, (b) after combining R_3 and R_4 in parallel and combining R_2 and R_5 in series, and (c) after combining the 3 Ω and 6 Ω resistances in parallel.

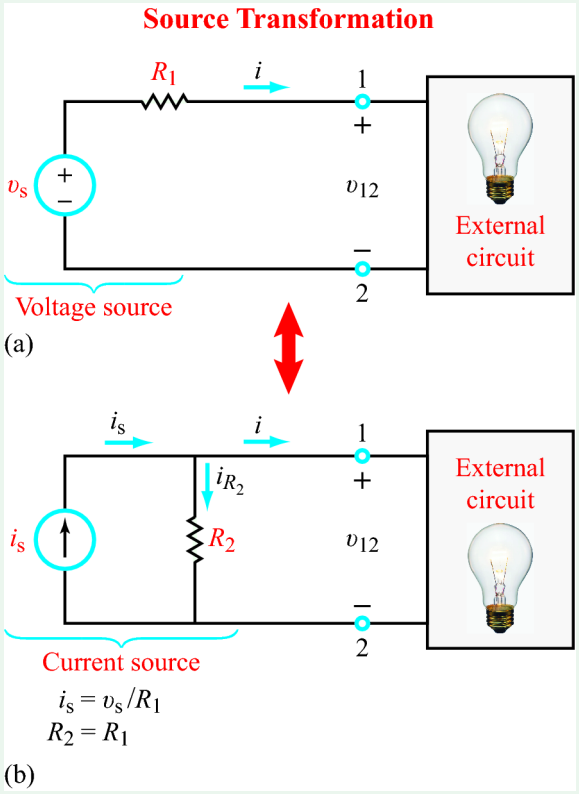


Figure 2.29 Realistic voltage and current sources connected to an external circuit. Equivalence requires that $i_s = v_s/R_1$ and $R_2 = R_1$.

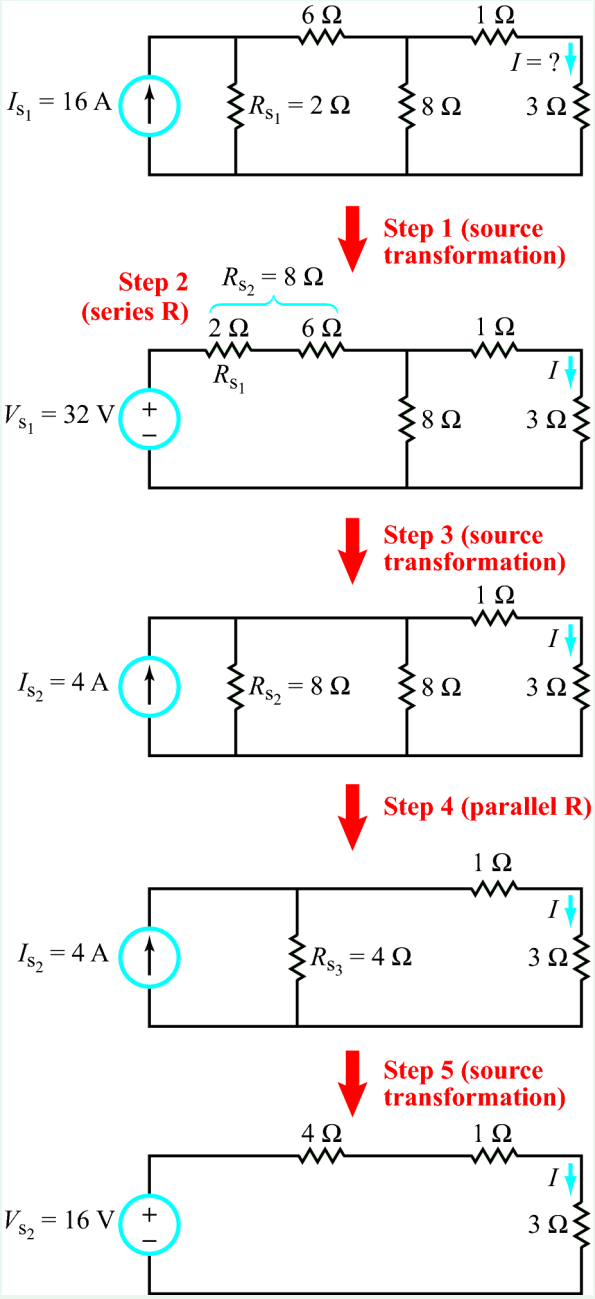


Figure 2.30 Example 2-13 circuit evolution.

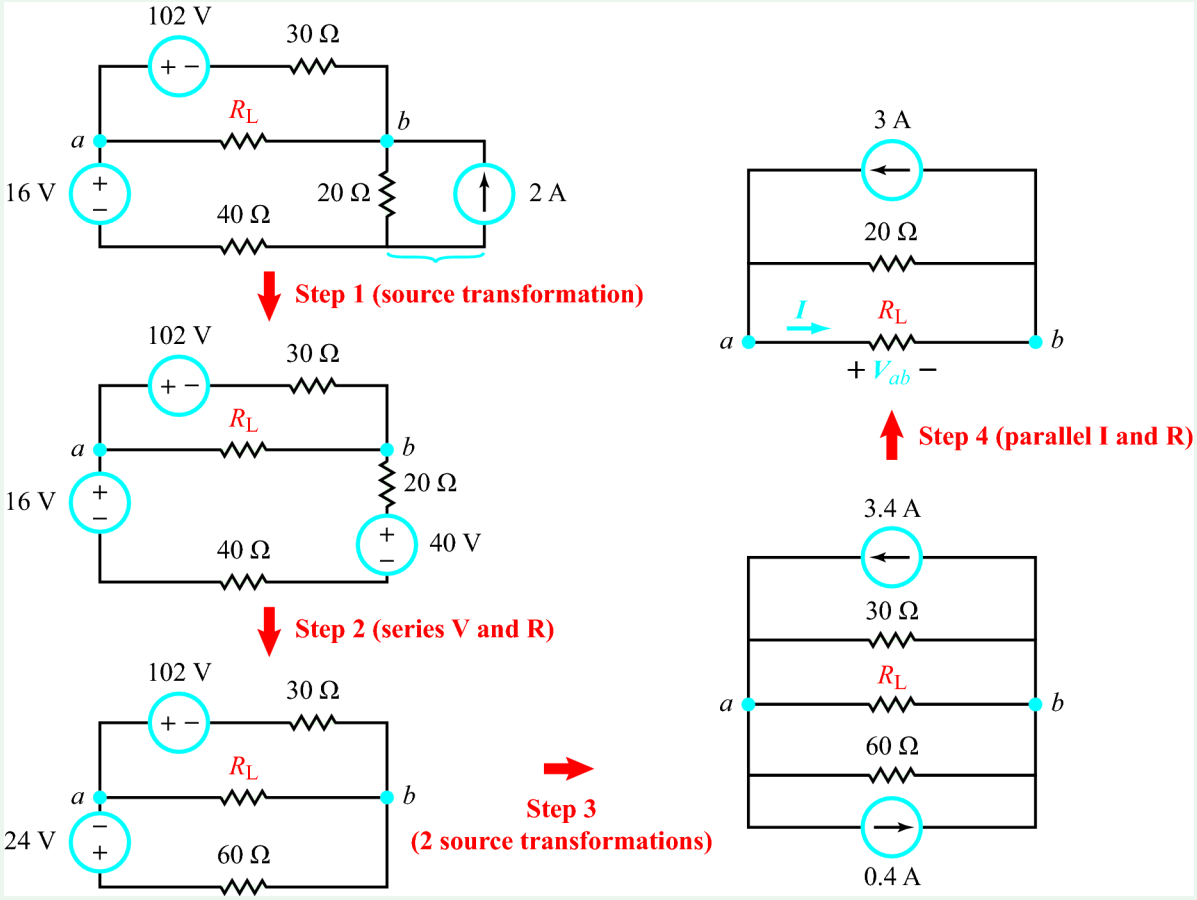


Figure 2.31 Circuit evolution for Example 2-14.

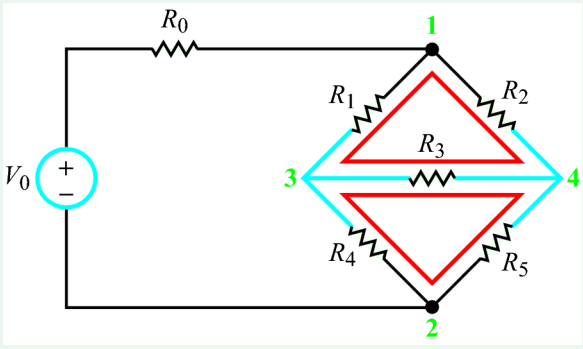


Figure 2.32 No two resistors of this circuit share the same current (connected in series) or voltage (connected in parallel).

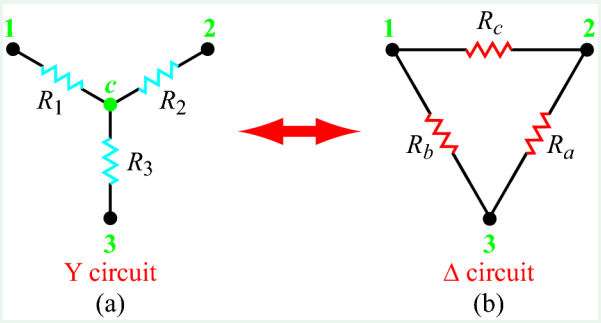


Figure 2.33 Y–Δ equivalent circuits.

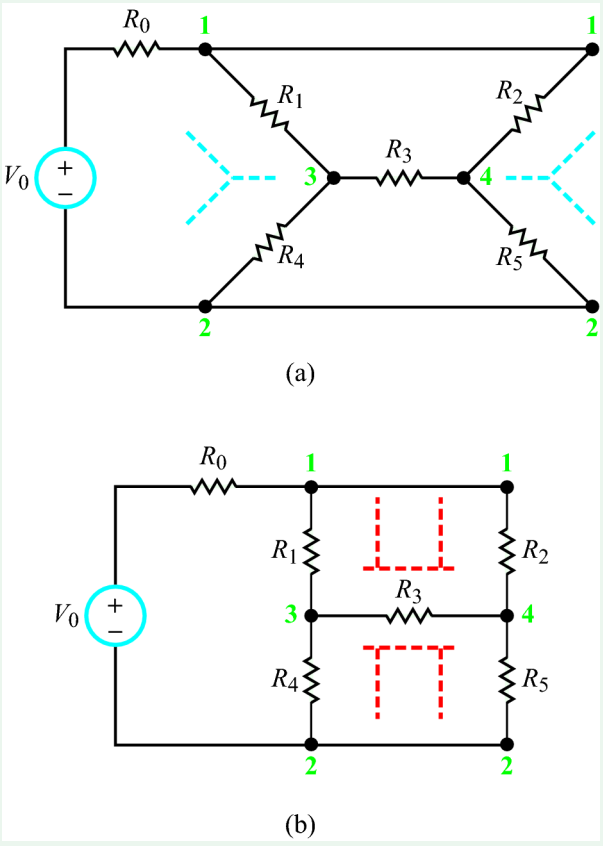


Figure 2.34 Redrawing the circuit of **Fig.** 2.32 to resemble (a) Y and (b) T and Π subcircuits.

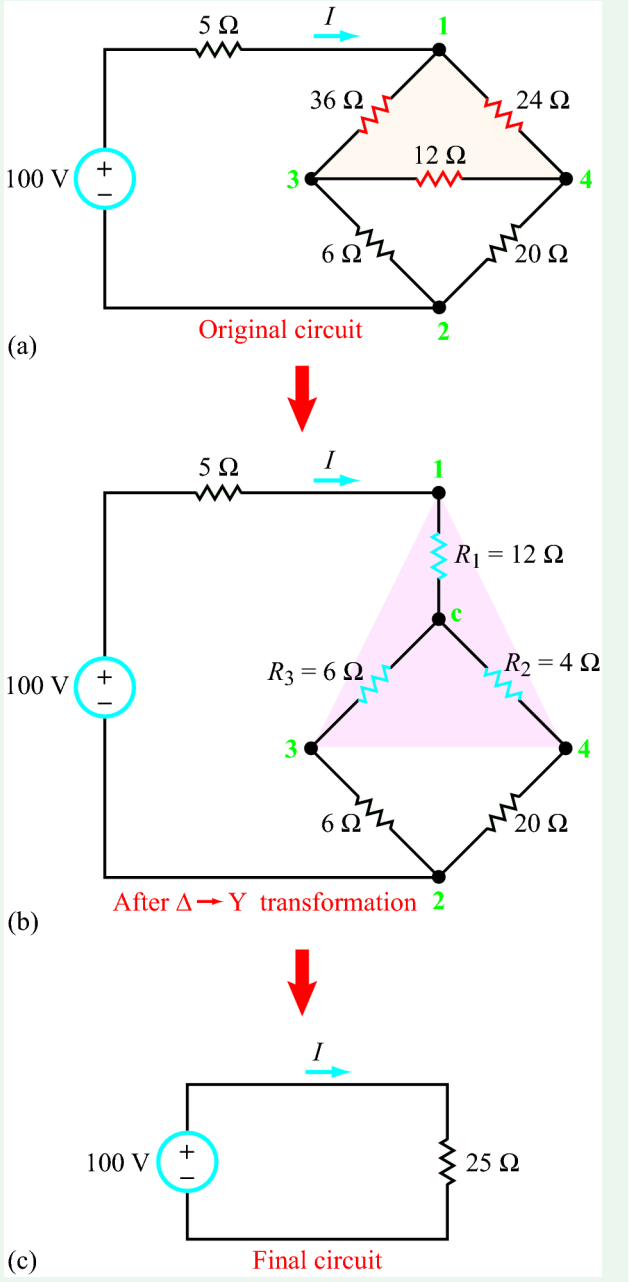


Figure 2.35 Example 2-15 circuit evolution.

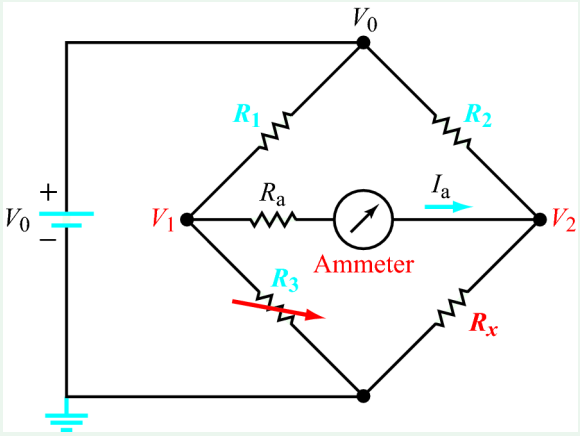
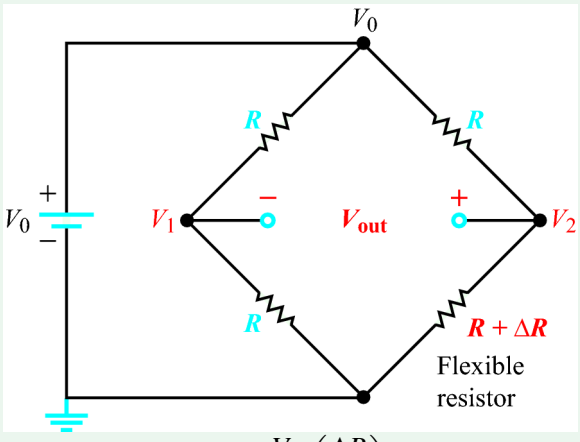


Figure 2.36 Wheatstone-bridge circuit containing an adjustable variable resistor R_3 and an unknown resistor R_x. When R_3 is adjusted to make $I_a = 0$, R_x is determined from $R_x = (R_2/R_1)R_3$.



$$V_{out} \approx \frac{V_0}{4}\left(\frac{\Delta R}{R}\right)$$

Figure 2.37 Circuit for Wheatstone-bridge sensor.

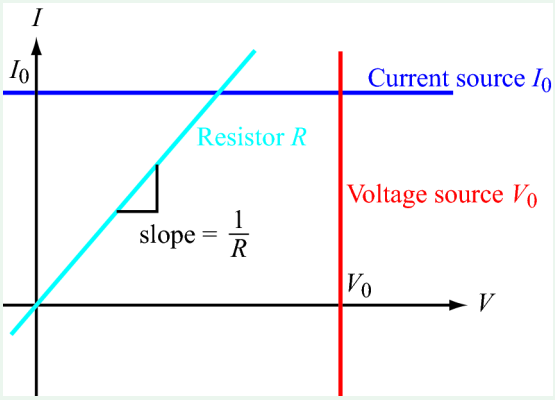
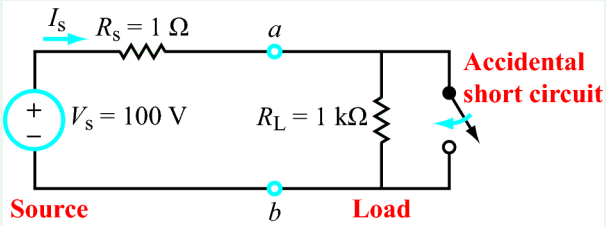
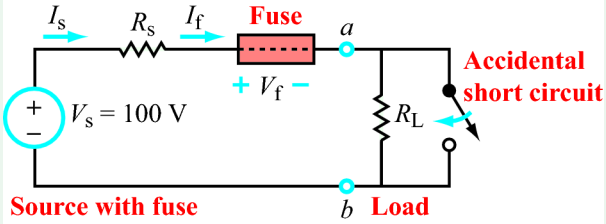


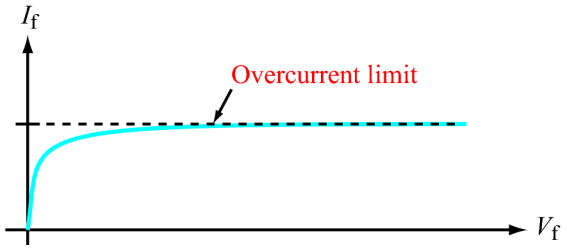
Figure 2.38 *I–V* relationships for a resistor R, an ideal voltage source V_0, and an ideal current source I_0.



(a) Accidental short circuit represented by a switch



(b) Fuse to protect voltage source



(c) *i–v* characteristic for a fuse prior to opening

Figure 2.39 Use of a fuse to protect a voltage source.

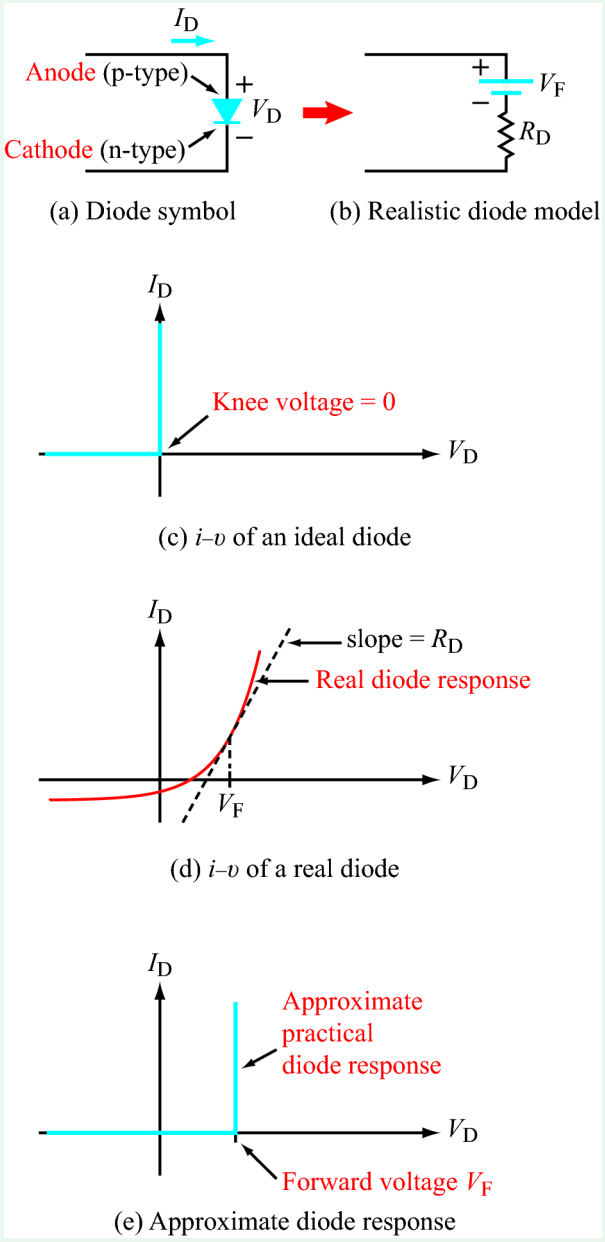


Figure 2.40 pn-junction diode schematic symbol and i–v characteristics.

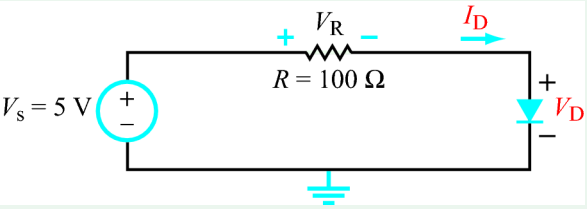


Figure 2.41 Diode circuit of Example 2-17.

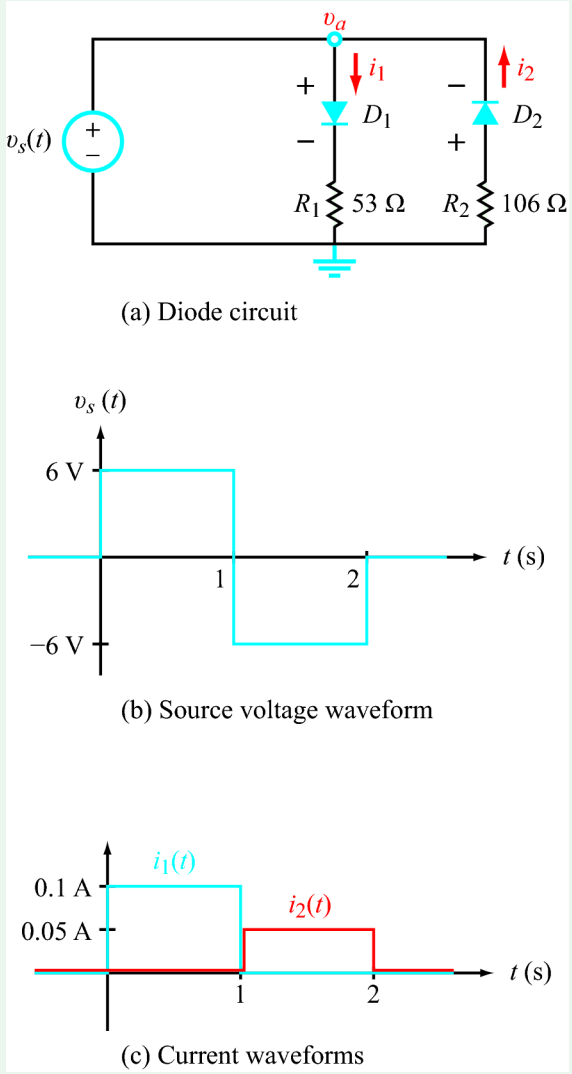


Figure 2.42 Diode circuit and waveforms of Example 2-18.

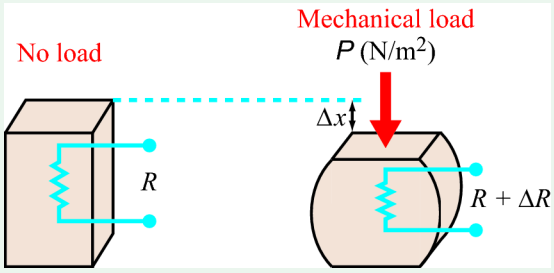


Figure 2.43 The resistance of a piezoresistor changes when mechanical stress is applied.

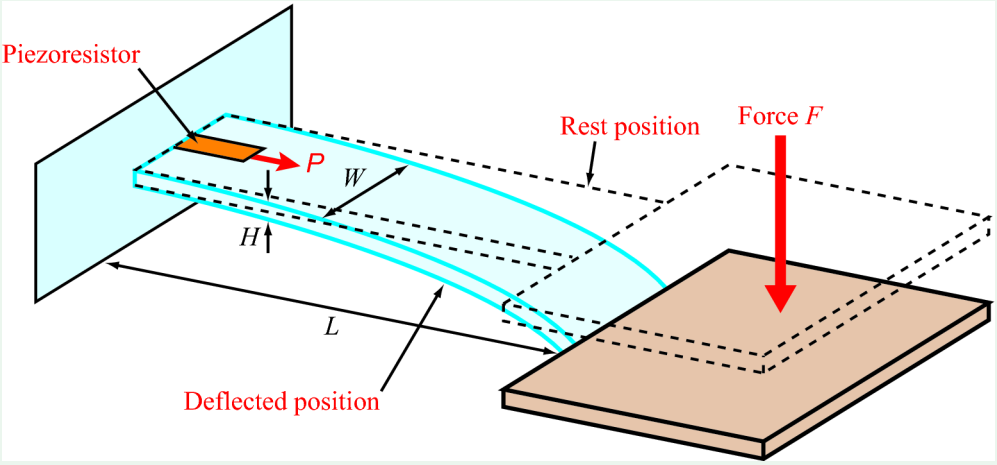


Figure 2.44 A cantilever structure with integrated piezoresistor at the base.

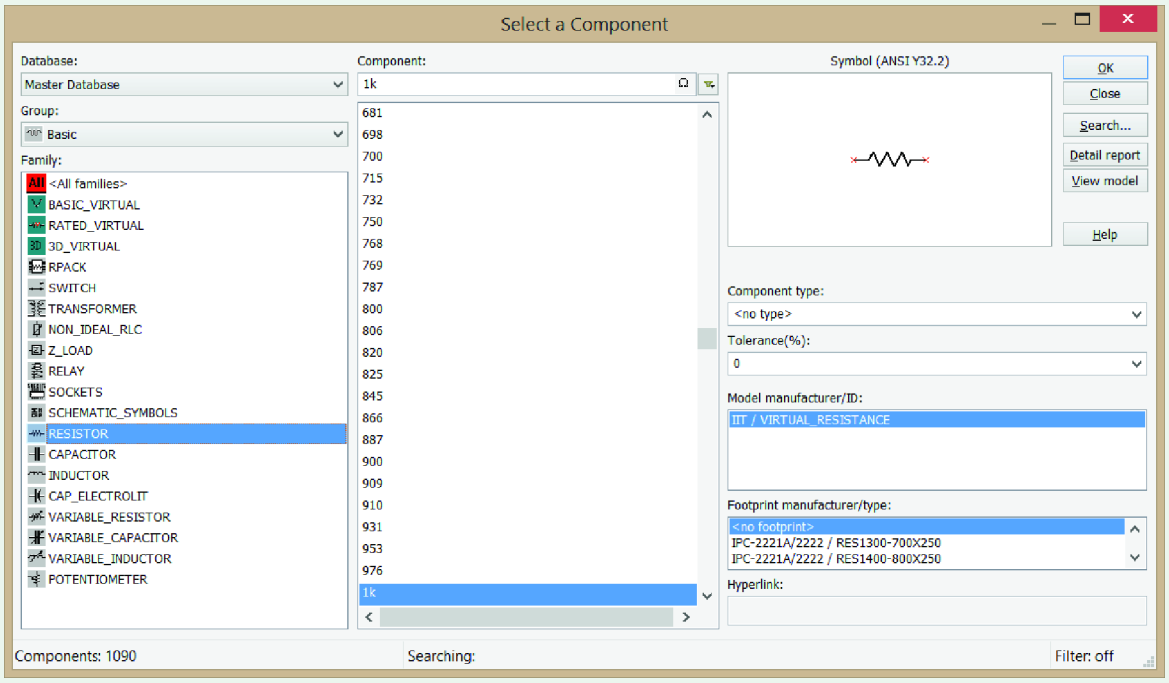


Figure 2.45 Multisim screen for selecting and placing a resistor.

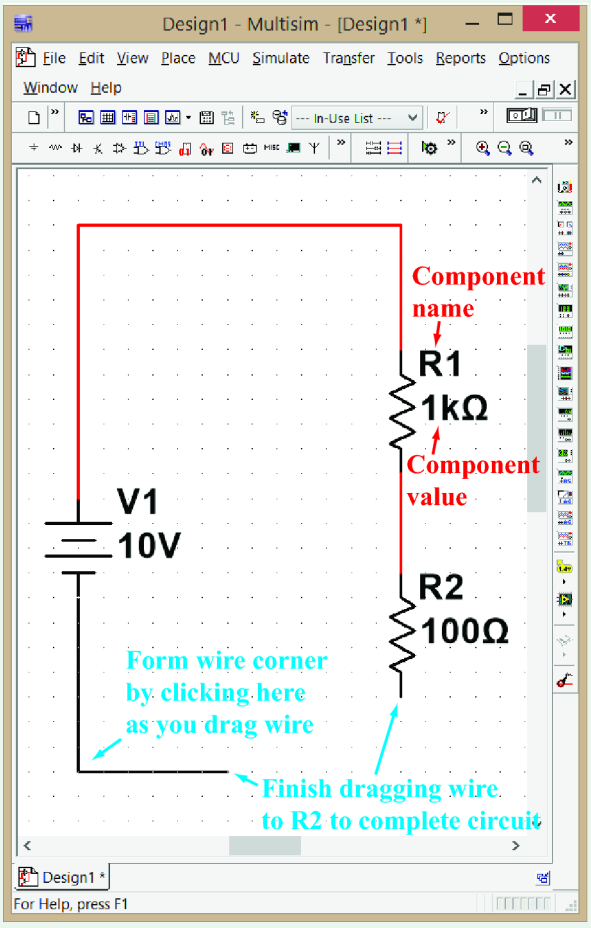


Figure 2.46 Adding a voltage source and completing the circuit.

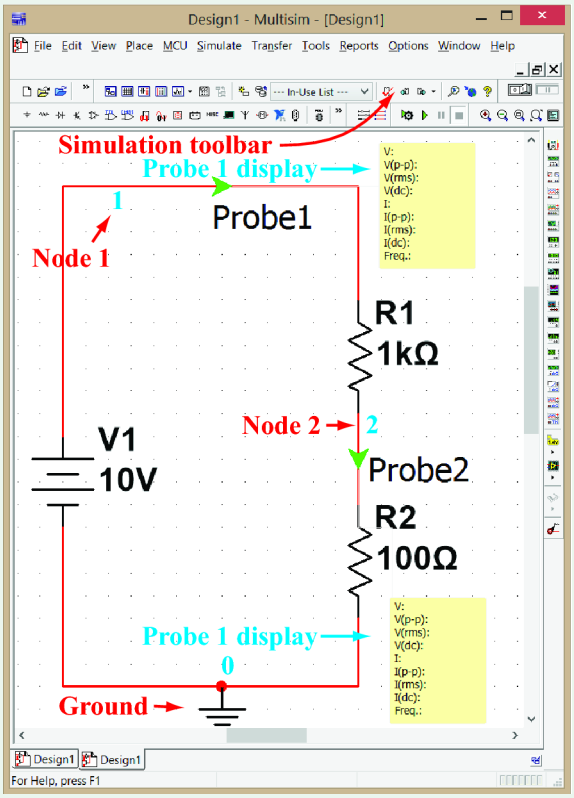


Figure 2.47 Executing a simulation.

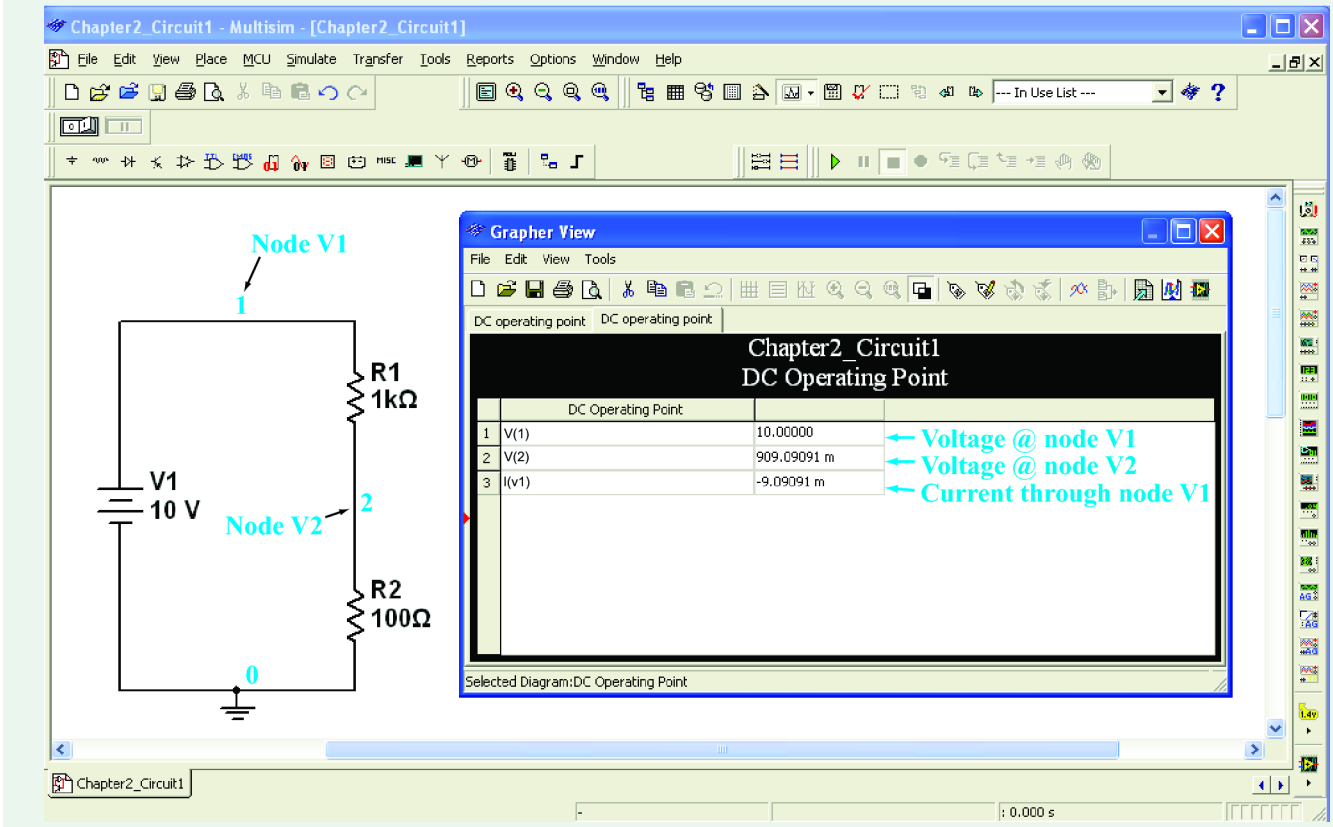


Figure 2.48 Solution window.

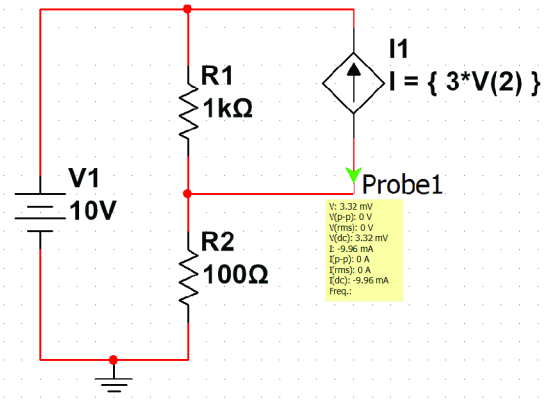


Figure 2.49 Creating a dependent source.

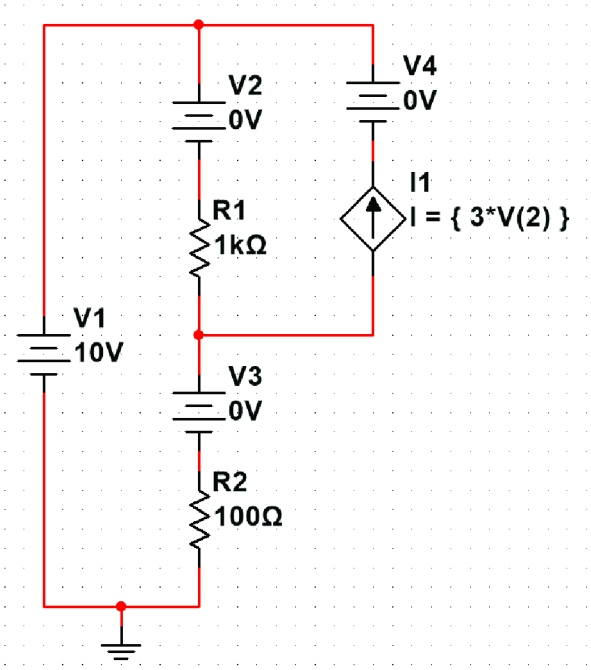


Figure 2.50 Circuit from **Fig.** 2.49 adapted to read out the currents through R1, R2, and the dependent source.

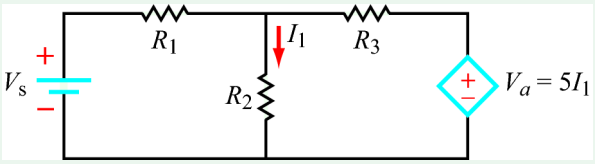


Figure 3.1 Circuit with dependent source $V_a = 5I_1$.

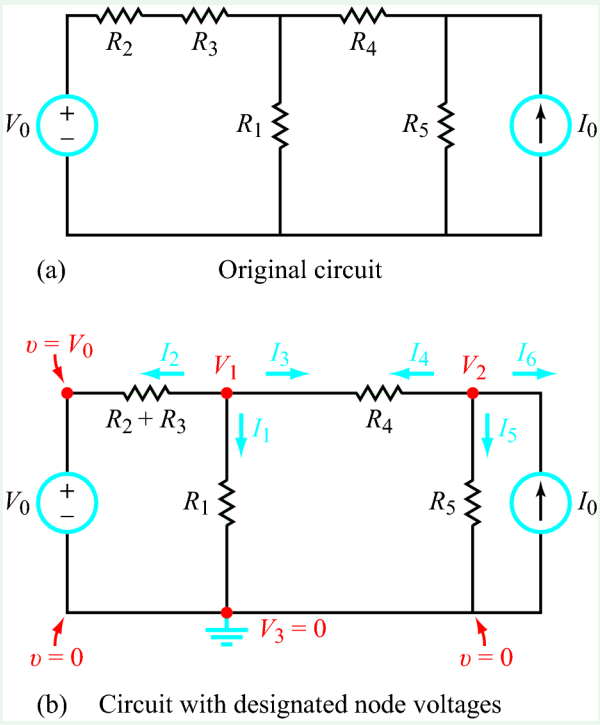
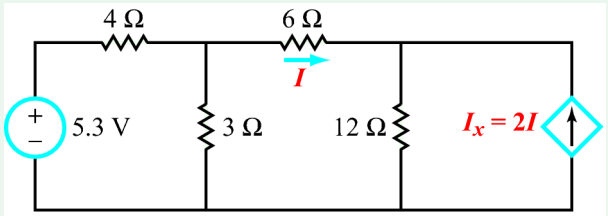
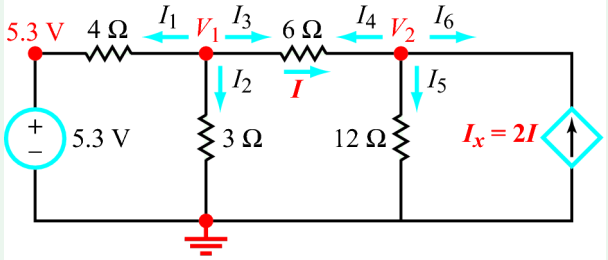


Figure 3.2 Circuit for Example 3-1.



(a) Original circuit



(b) Circuit with designated node voltages

Figure 3.3 Example 3-2.

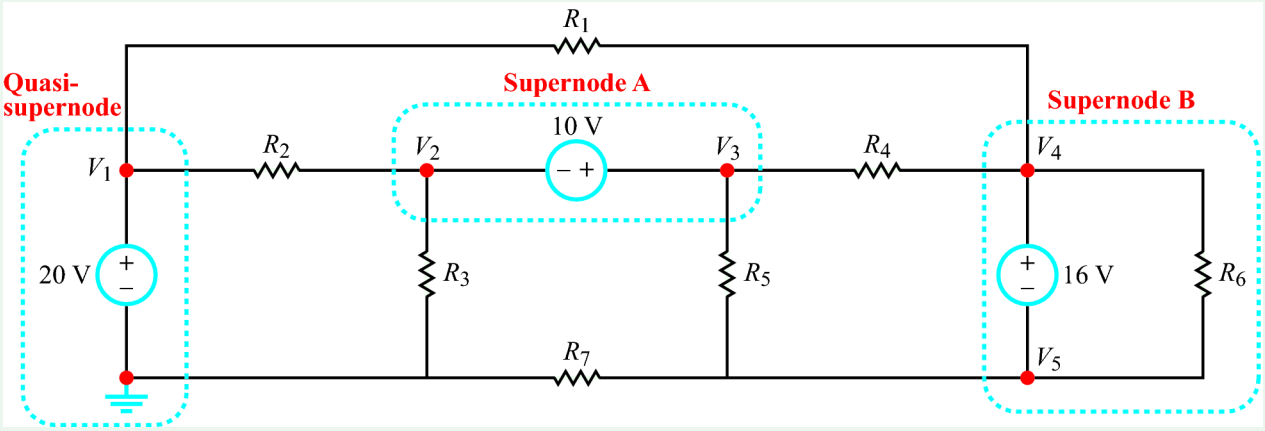


Figure 3.4 Circuit containing two supernodes and one quasi-supernode.

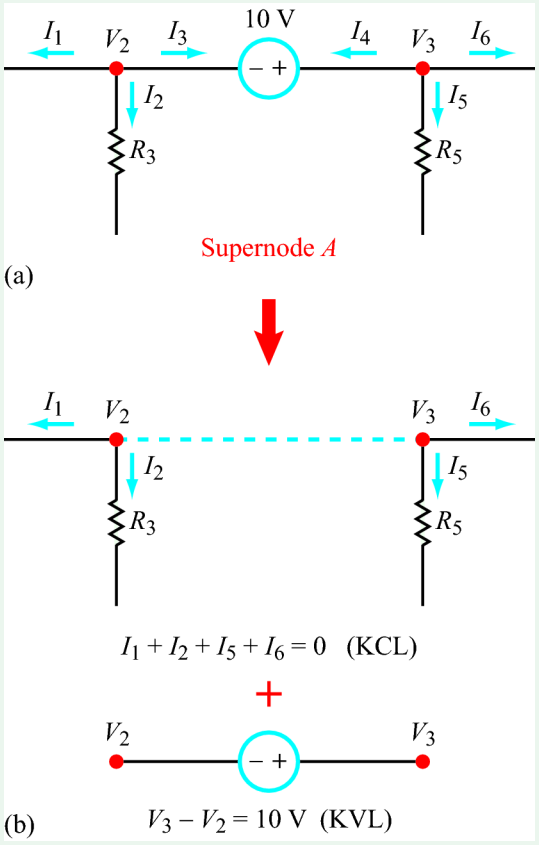


Figure 3.5 A supernode composed of nodes V_2 and V_3 can be represented as a single node, in terms of summing currents flowing out of them, plus an auxiliary equation that defines the voltage difference between V_3 and V_2.

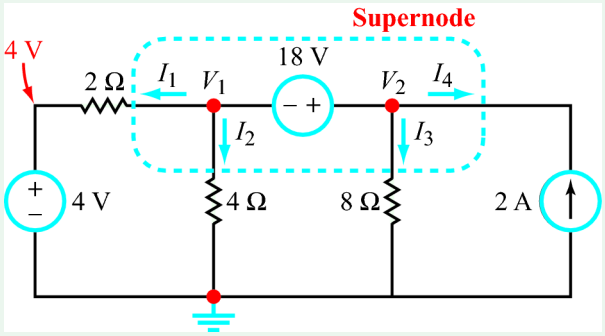


Figure 3.6 Circuit for Example 3-3.

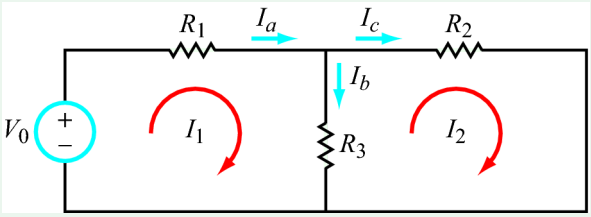


Figure 3.7 Circuit containing two meshes with mesh currents I_1 and I_2.

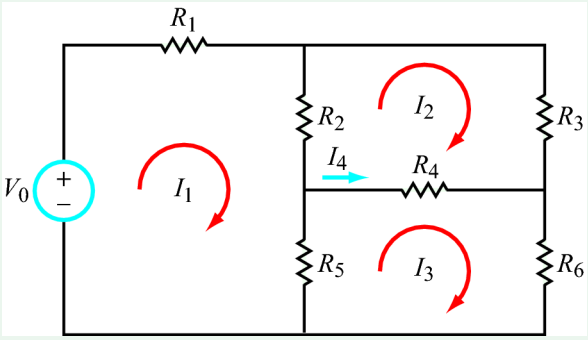


Figure 3.8 Circuit for Example 3-4.

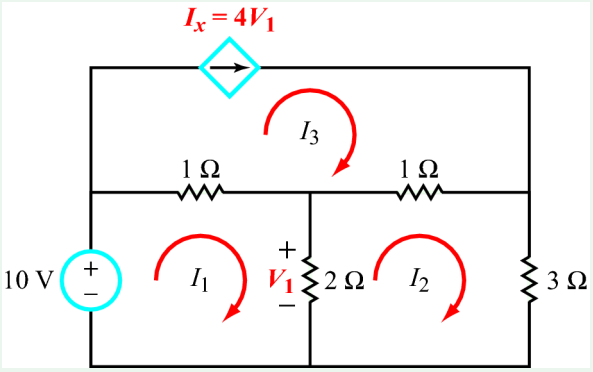
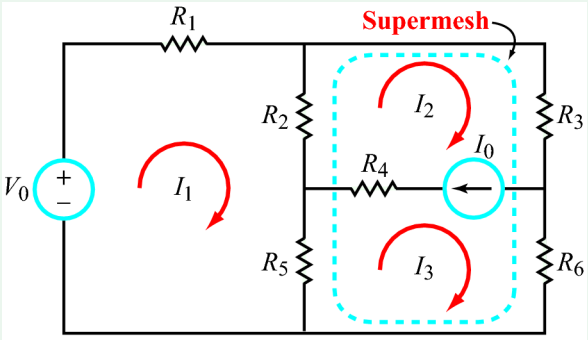
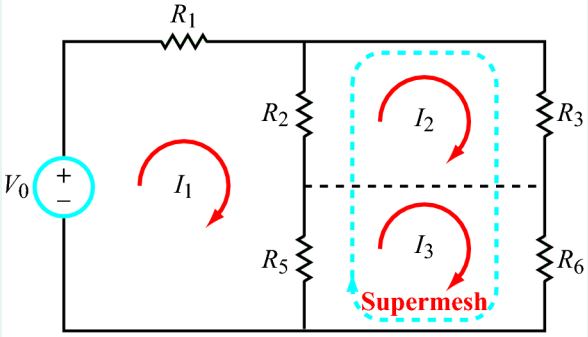


Figure 3.9 Mesh-current solution for a circuit containing a dependent source (Example 3-5).

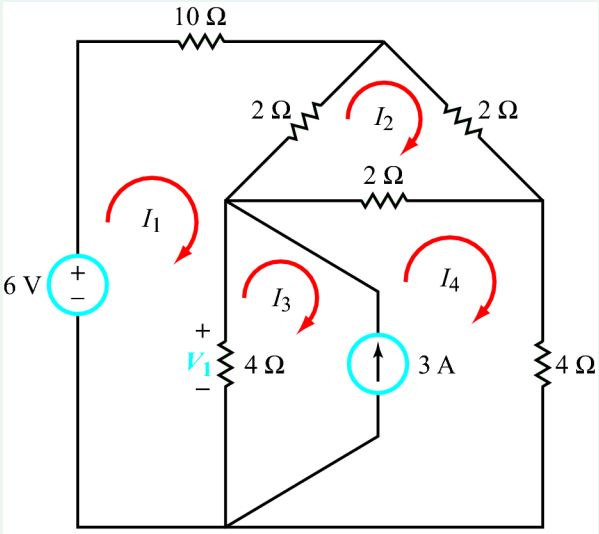


(a) Two adjoining meshes sharing a current source constitute a supermesh.

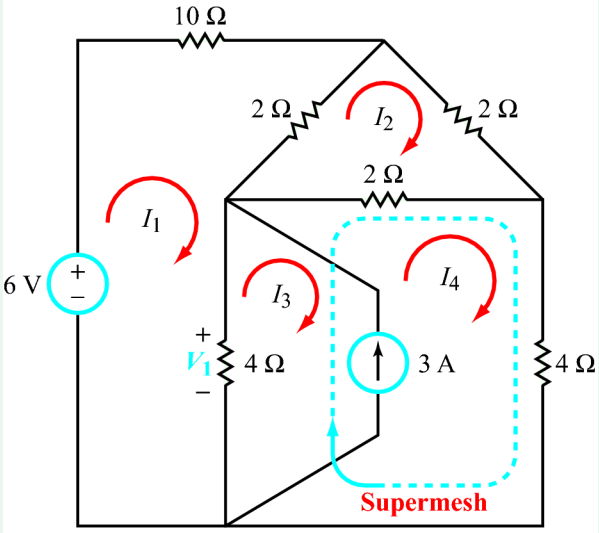


(b) Meshes 2 and 3 can be combined into a single supermesh equation, plus an auxiliary equation $I_0 = I_2 - I_3$.

Figure 3.10 Concept of a supermesh.

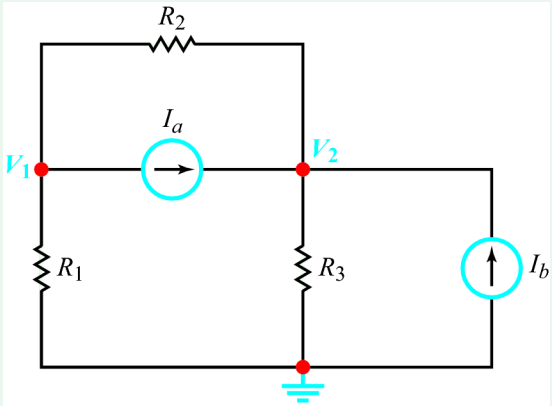


(a) Original circuit

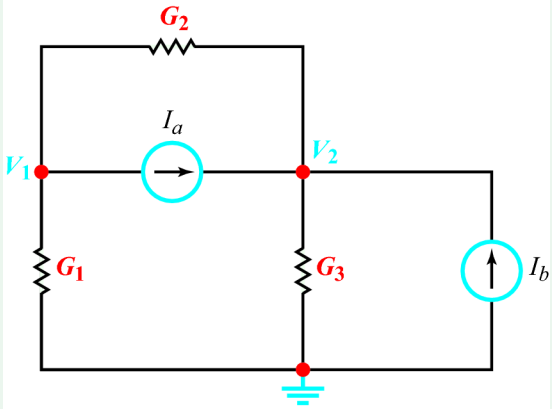


(b) Meshes 3 and 4 constitute a supermesh

Figure 3.11 Using the supermesh concept to simplify solution of the circuit in Example 3-6.



(a) Original circuit



(b) Circuit in terms of conductances

Figure 3.12 Application of the nodal-analysis by-inspection method is facilitated by replacing resistors with conductances.

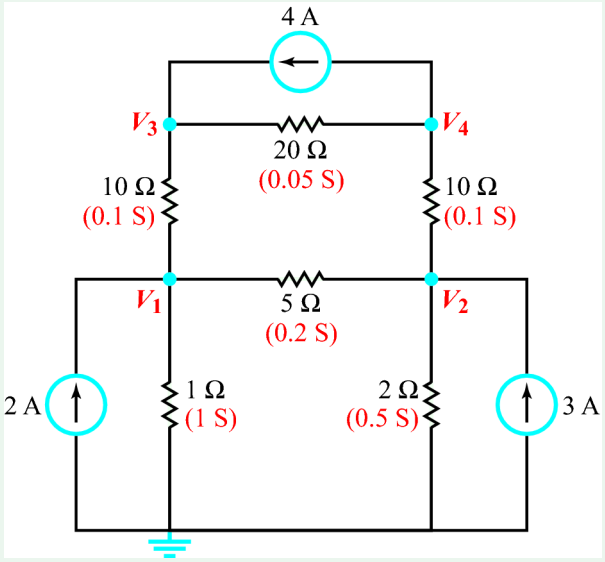


Figure 3.13 Circuit for Example 3-7.

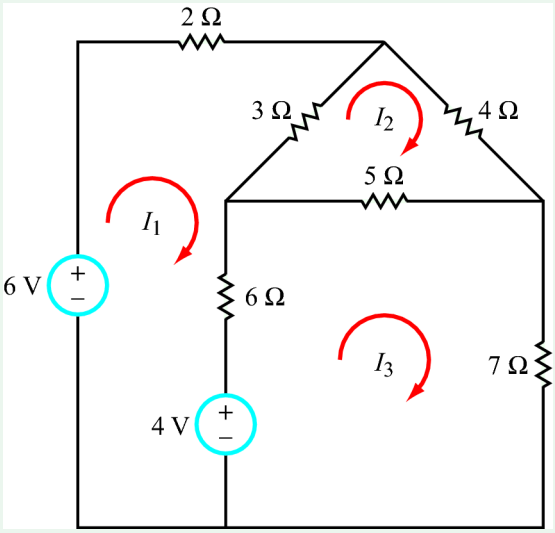
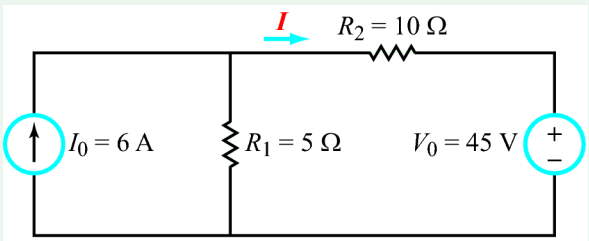
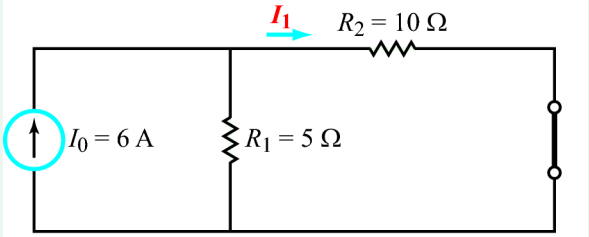


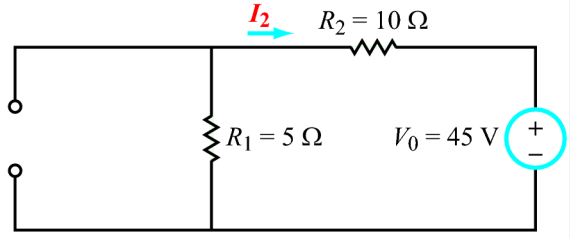
Figure 3.14 Three-mesh circuit of Example 3-8.



(a) Original circuit



(b) Source I_0 alone generates I_1
[Eliminating a voltage source = replacing it with short circuit]



(c) Source V_0 alone generates I_2
[Eliminating a current source = replacing it with open circuit]

Figure 3.15 Application of the source-superposition method to the circuit of Example 3-9.

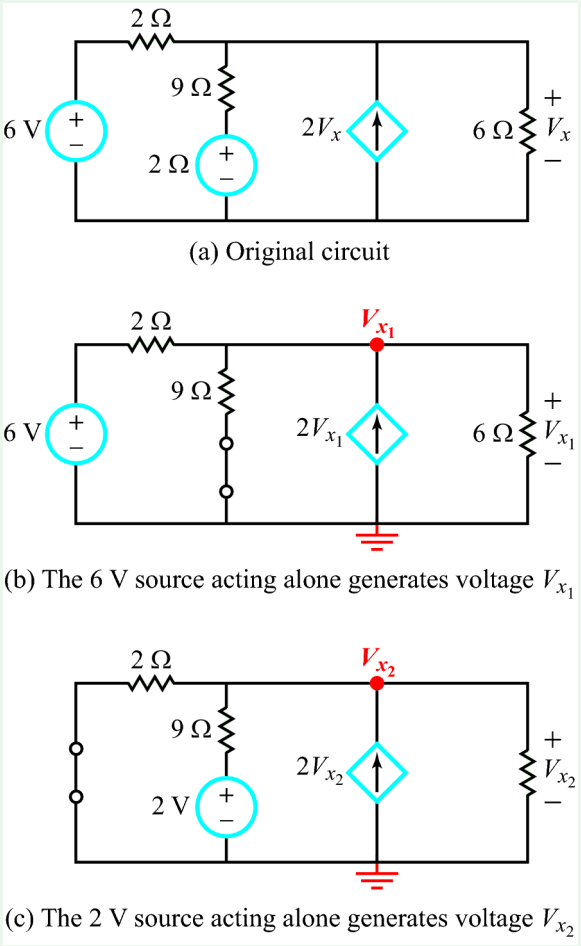


Figure 3.16 Application of superposition to the circuit of Example 3-10.

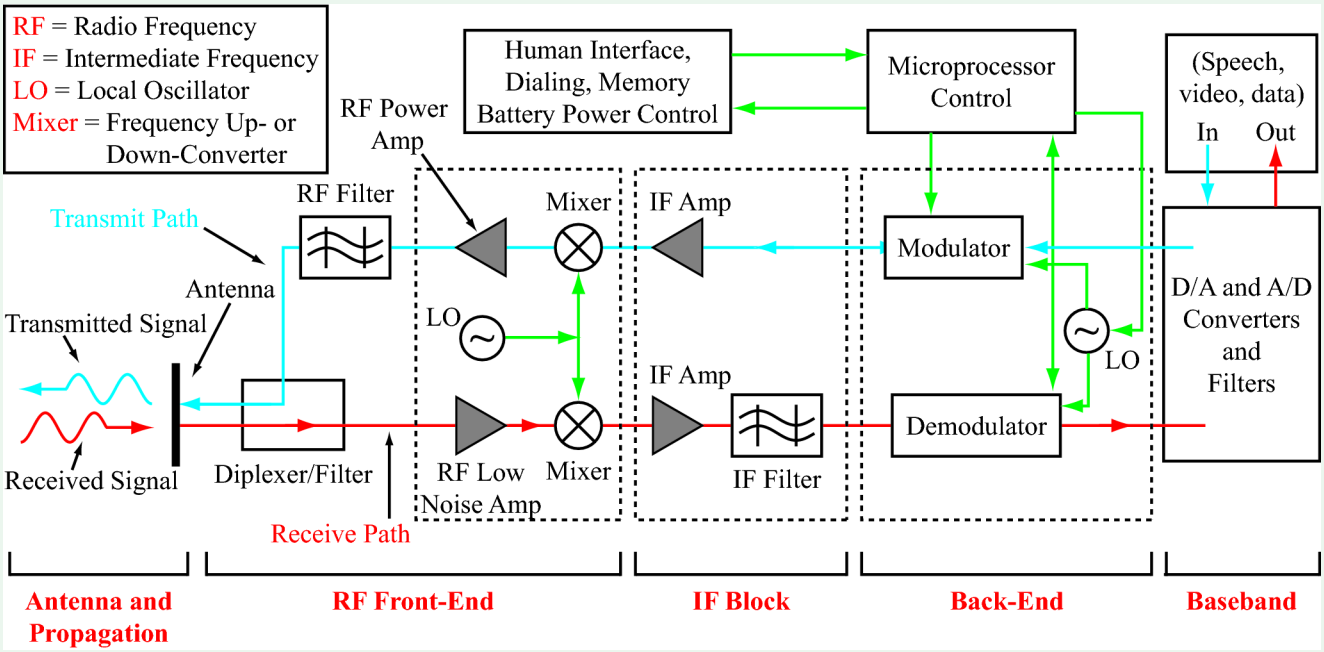


Figure 3.17 Cell-phone block diagram.

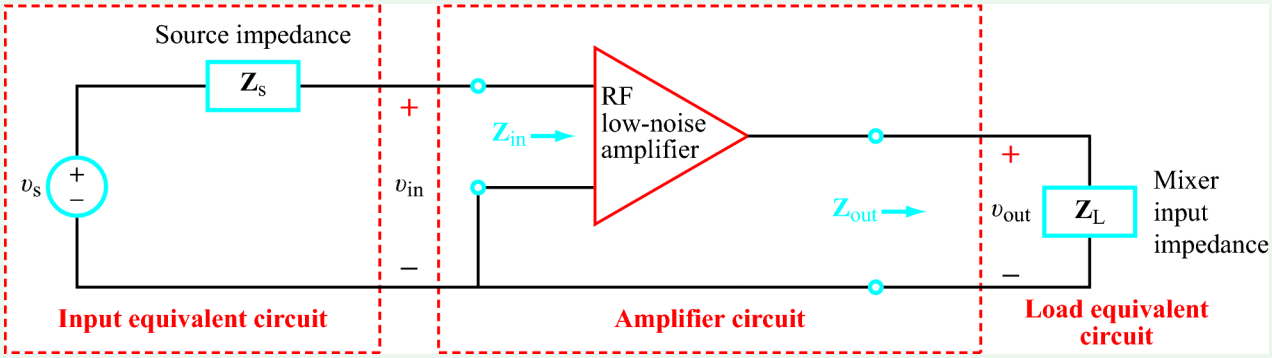


Figure 3.18 Input and output circuits as seen from the perspective of a radio-frequency amplifier circuit.

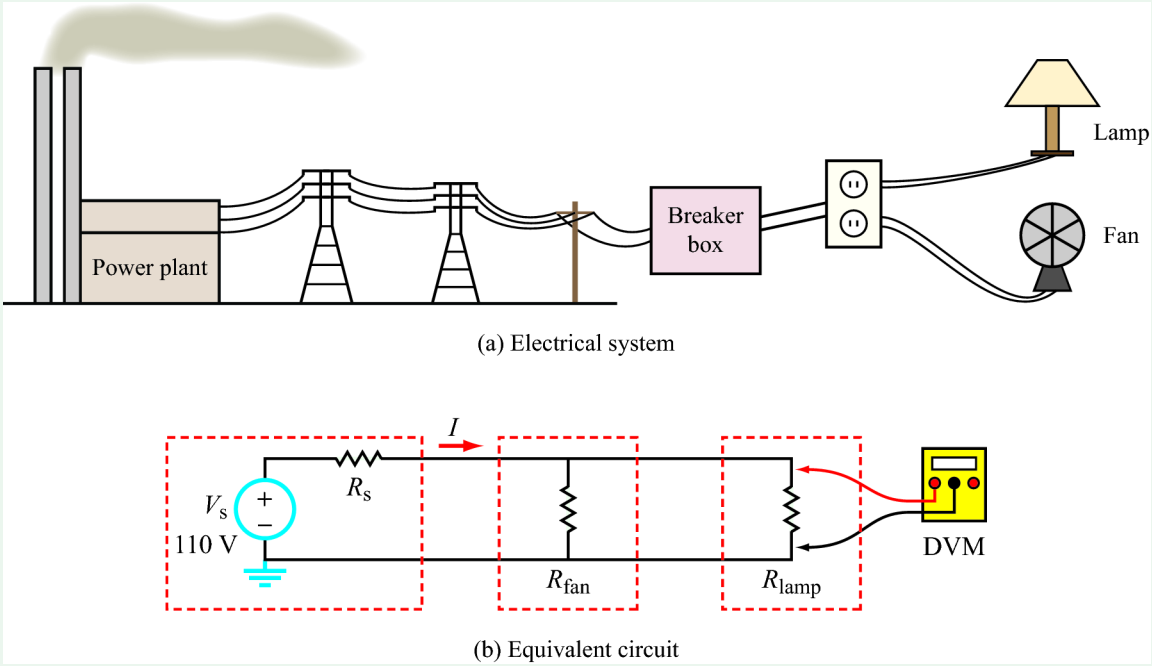


Figure 3.19 (a) Power distribution system driving a fan and a lamp in a house, and (b) block diagram of the source (power distribution system), fan, lamp, and a voltmeter measuring the voltage in the outlet.

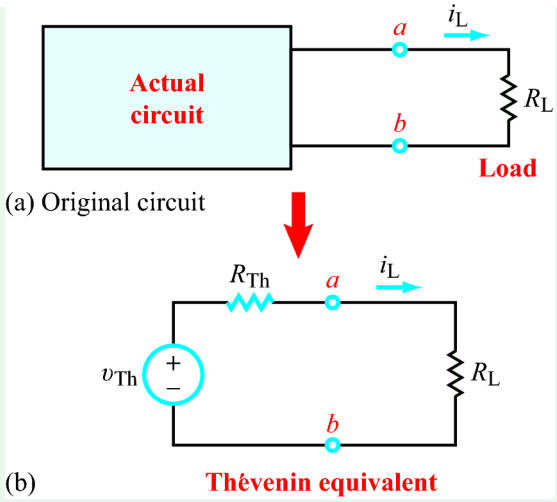


Figure 3.20 A circuit can be represented in terms of a Thévenin equivalent comprising a voltage source v_{Th} in series with a resistance R_{Th}.

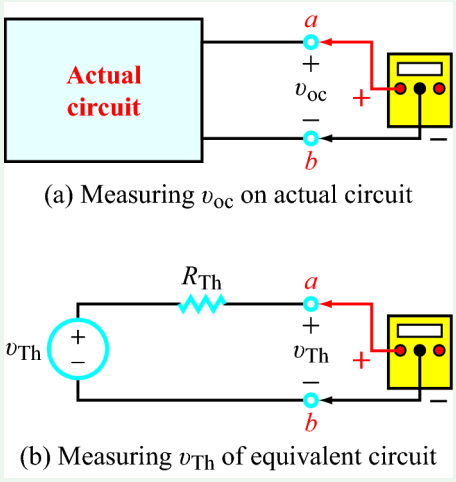


Figure 3.21 Equivalency means that v_{Th} of the Thévenin equivalent circuit is equal to the open-circuit voltage for the actual circuit.

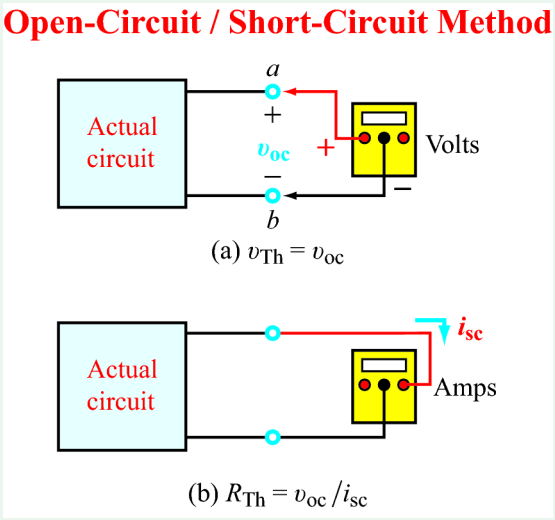


Figure 3.22 Thévenin voltage is equal to the open-circuit voltage and Thévenin resistance is equal to the ratio of v_{oc} to i_{sc}, where i_{sc} is the short-circuit current between the output terminals.

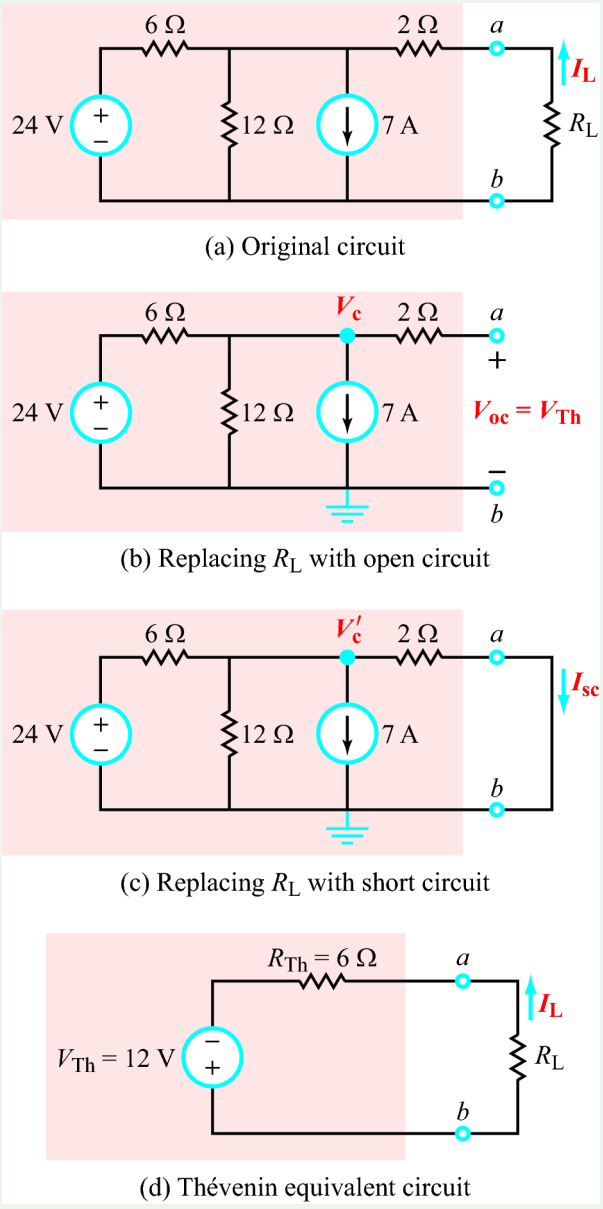


Figure 3.23 Applying open circuit/short circuit method to find the Thévenin equivalent for the circuit of Example 3-10.

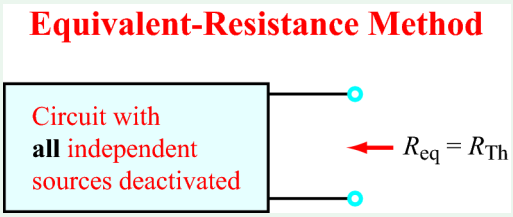


Figure 3.24 For a circuit that does not contain dependent sources, R_{Th} can be determined by deactivating all sources (replacing voltage sources with short circuits and current sources with open circuits) and then simplifying the circuit down to a single resistance R_{eq}.

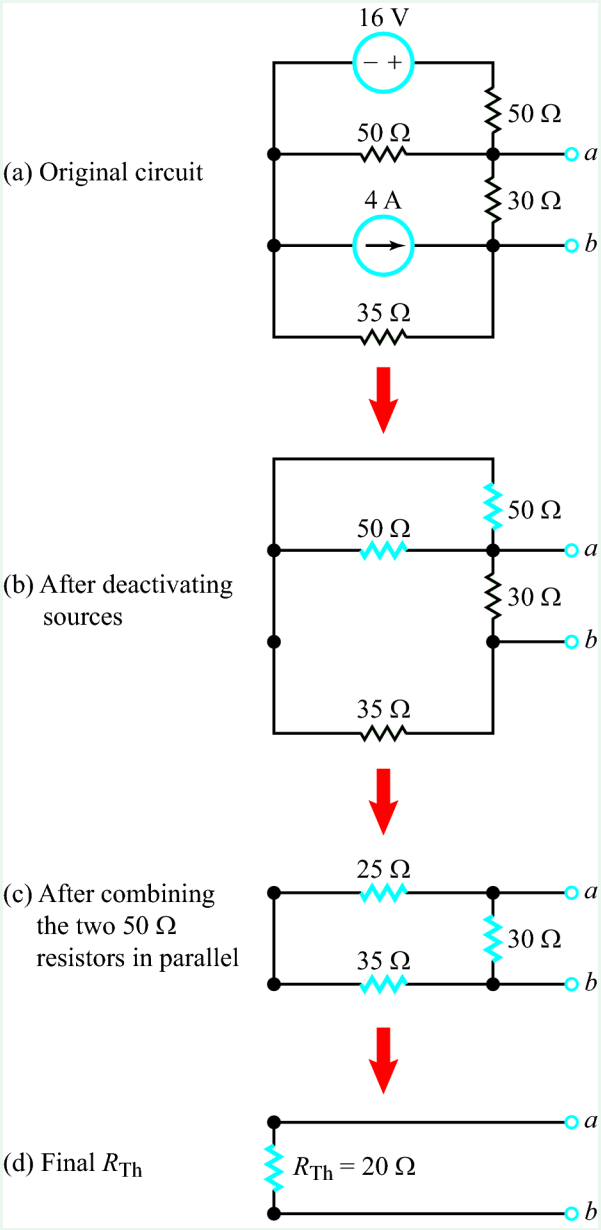


Figure 3.25 After deactivation of sources, systematic simplification leads to R_{Th} (Example 3-12).

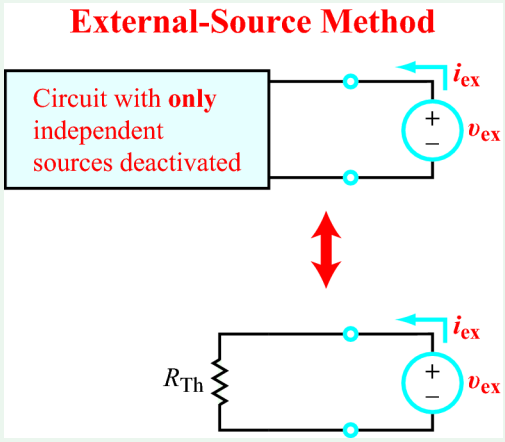


Figure 3.26 If a circuit contains both dependent and independent sources, R_{Th} can be determined by (a) deactivating only independent sources (by replacing independent voltage sources with short circuits and independent current sources with open circuits), (b) adding an external source v_{ex}, and then (c) solving the circuit to determine i_{ex}. The solution is $R_{Th} = v_{ex}/i_{ex}$.

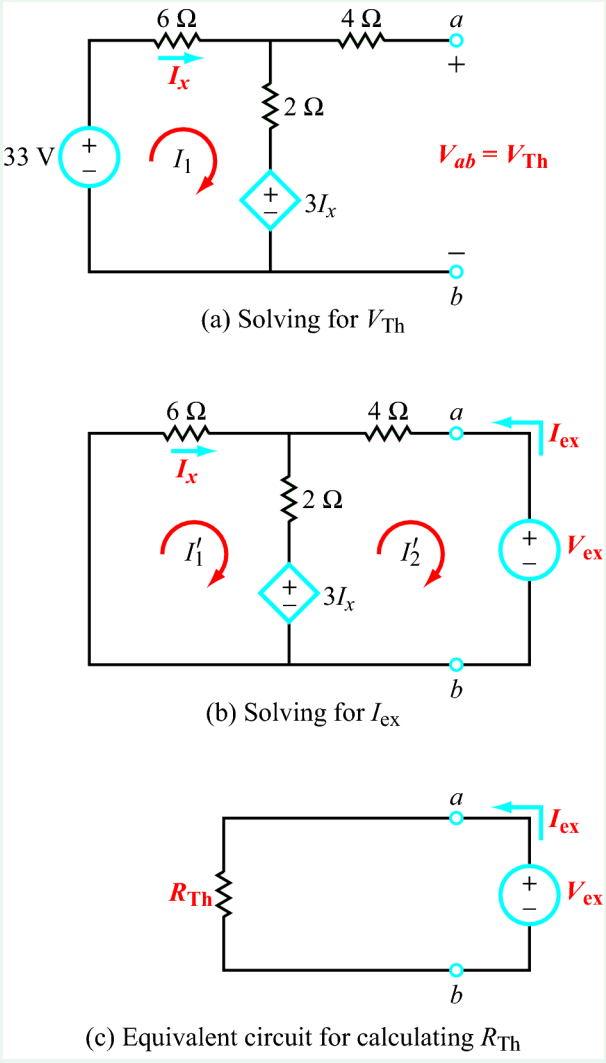


Figure 3.27 Solution of the open-circuit voltage gives $V_{ab} = V_{Th} = 15$ V. Use of the external-voltage method leads to $R_{Th} = 56/11\ \Omega$ (Example 3-13).

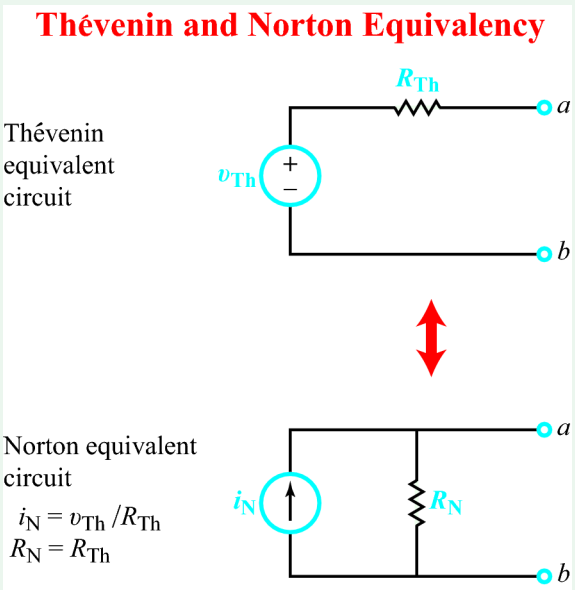


Figure 3.28 Equivalence between Thévenin and Norton equivalent circuits, consistent with the source transformation method of Section 2-3.4.

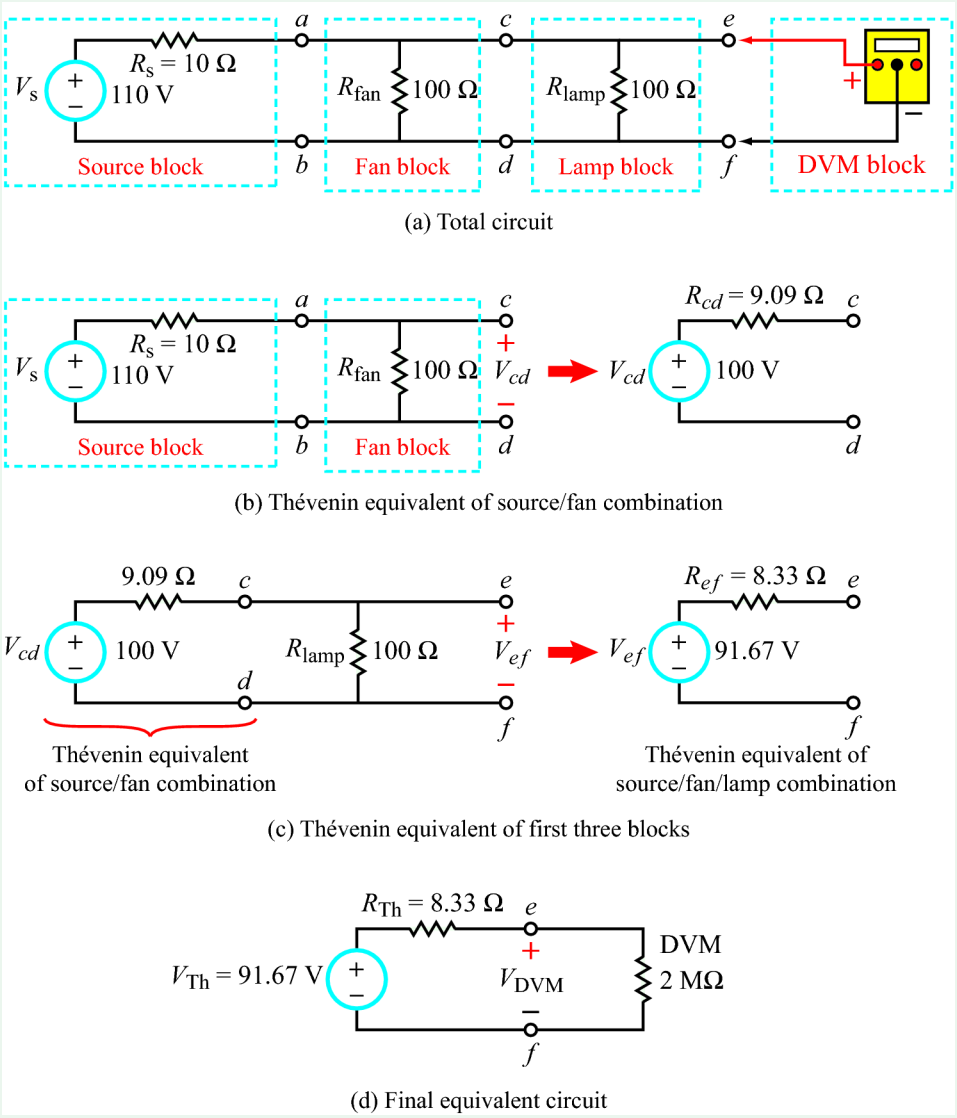


Figure 3.29 Repeated application of Thévenin-equivalent circuit technique.

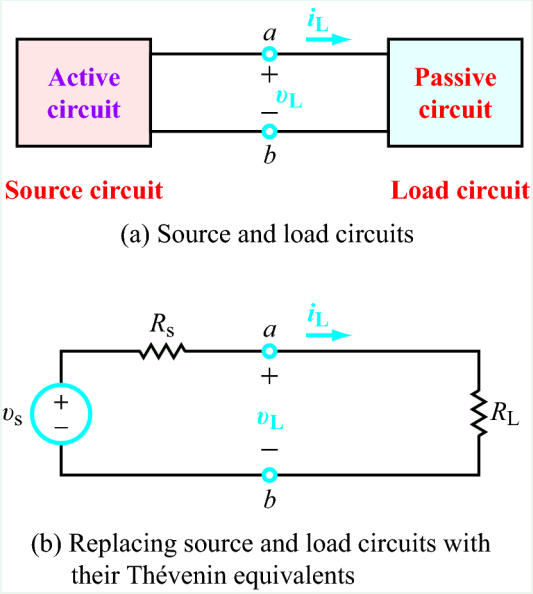


Figure 3.30 To analyze the transfer of voltage, current, and power from the source circuit to the load circuit, we first replace them with their Thévenin equivalents.

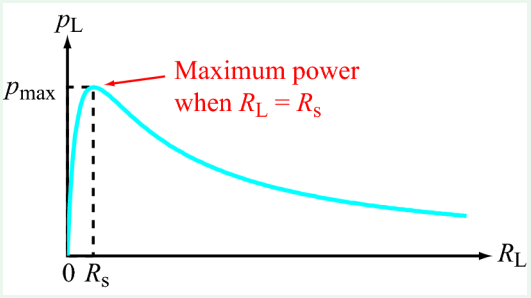


Figure 3.31 Variation of power p_L dissipated in the load R_L, as a function of R_L.

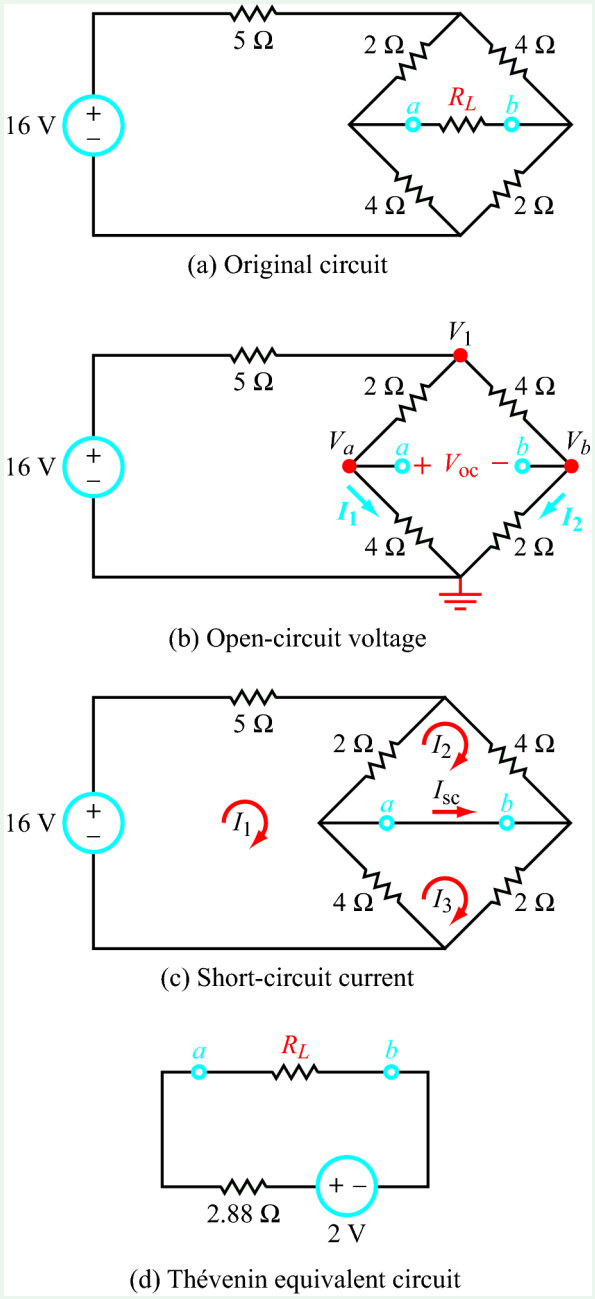


Figure 3.32 Evolution of the circuit of Example 3-15.

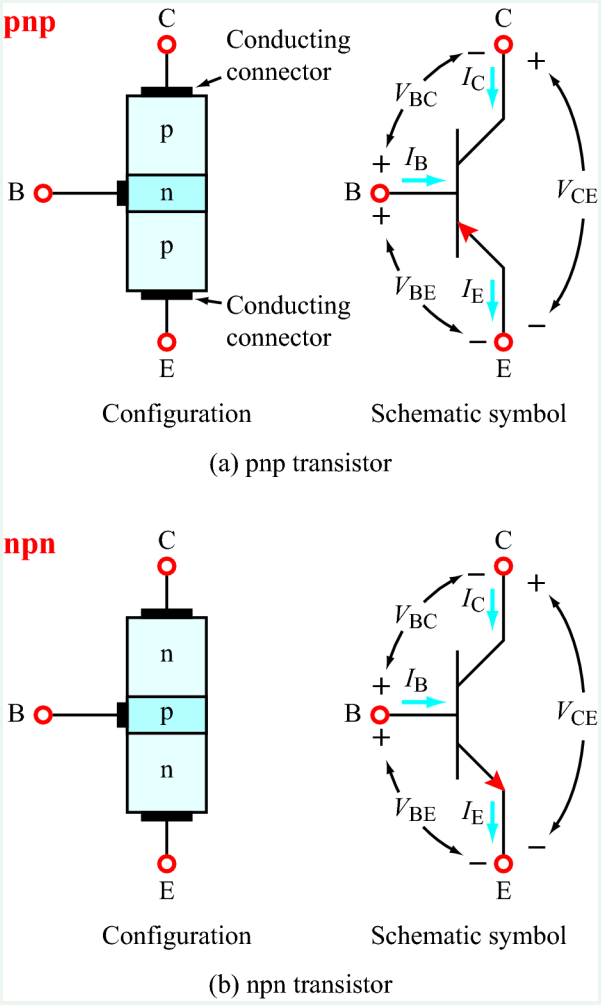


Figure 3.33 Configurations and symbols for (a) pnp and (b) npn transistors.

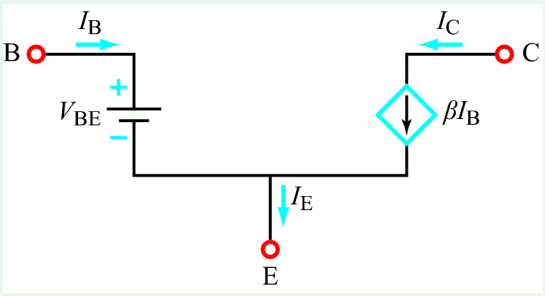


Figure 3.34 dc equivalent model for the npn transistor. The equivalent dc source $V_{BE} \approx 0.7$ V.

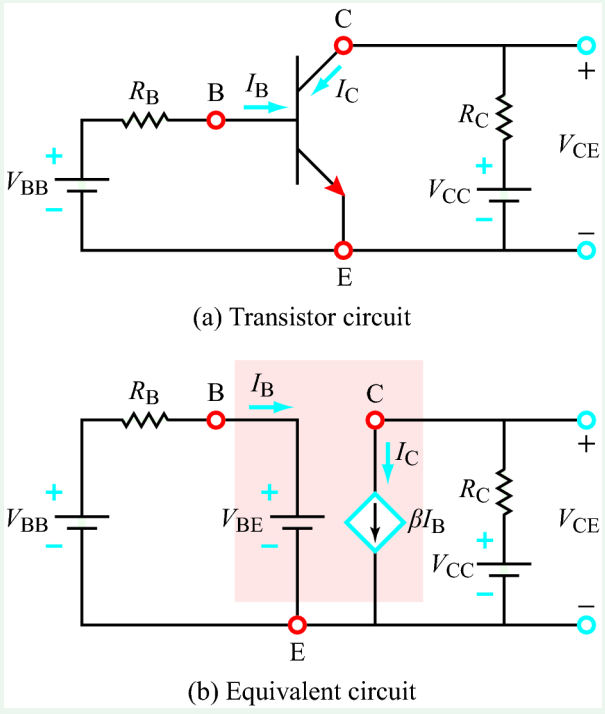


Figure 3.35 Circuit for Example 3-16.

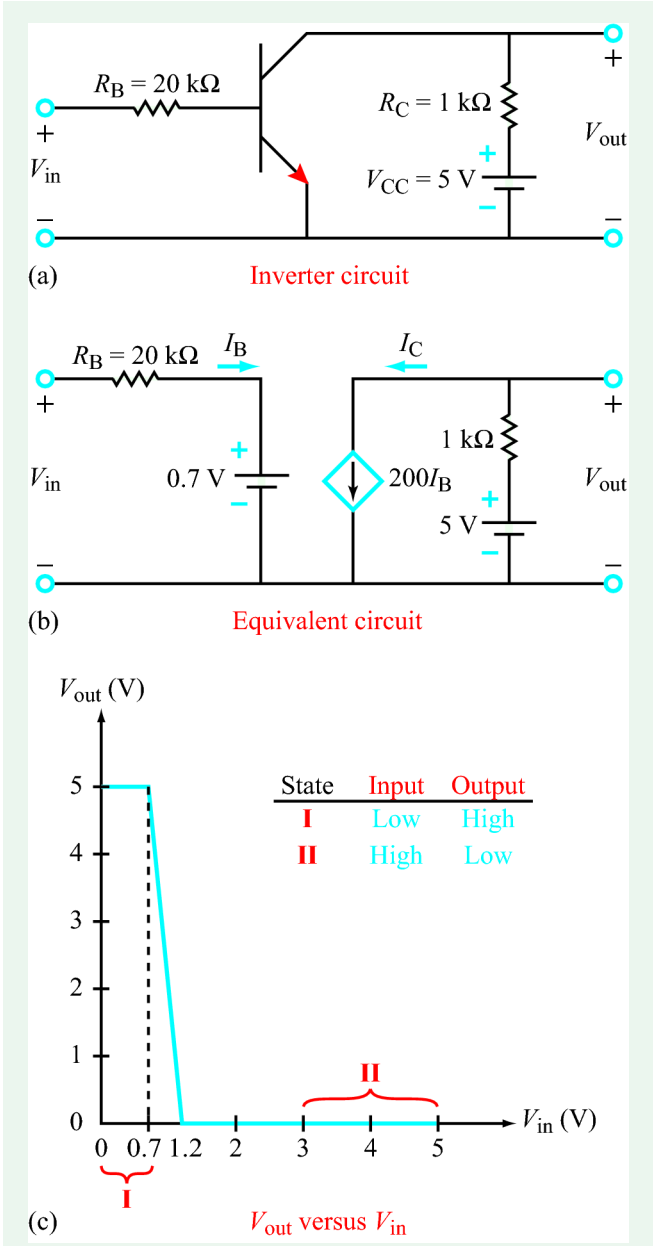
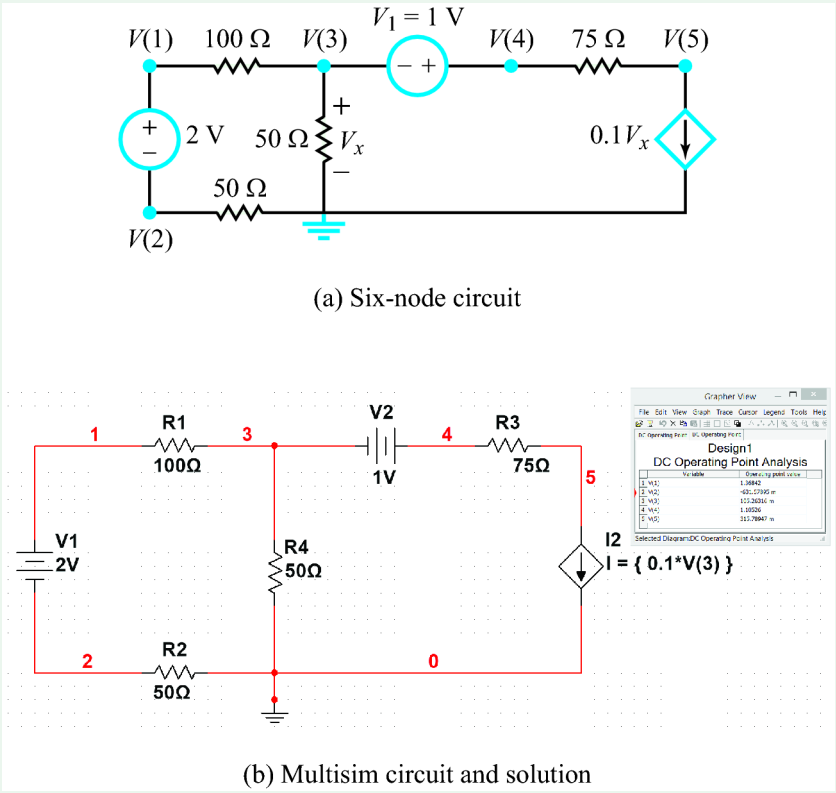


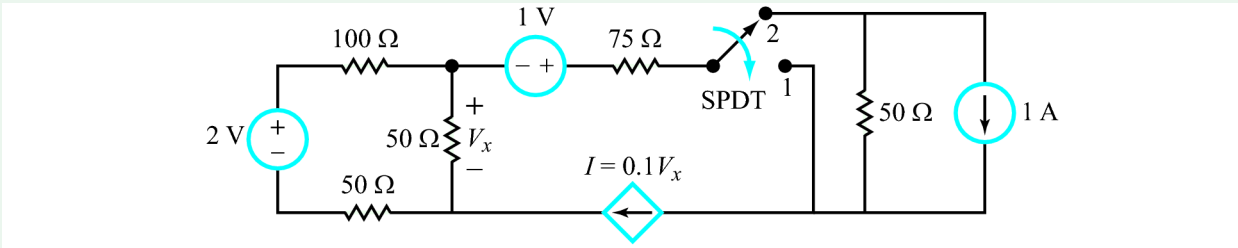
Figure 3.36 Circuit for Example 3-17.



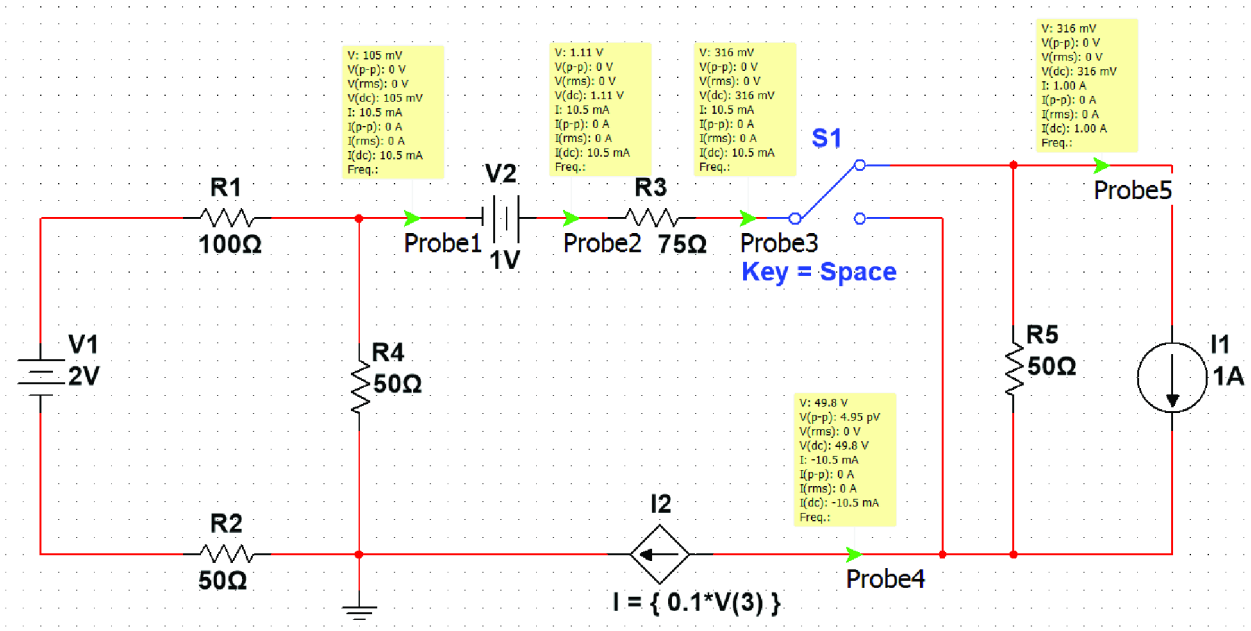
(a) Six-node circuit

(b) Multisim circuit and solution

Figure 3.37 Circuit analysis with Multisim.

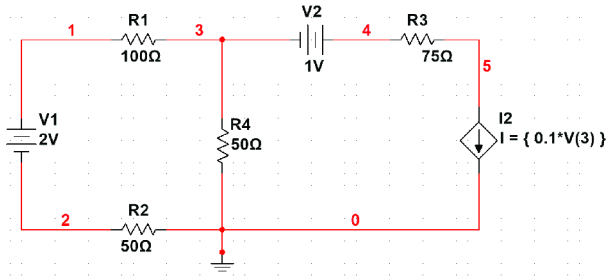


(a) Circuit with SPDT switch

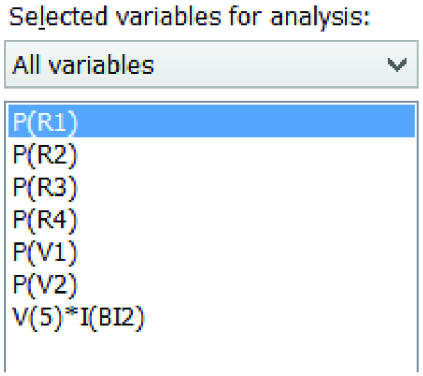


(b) Multisim configuration

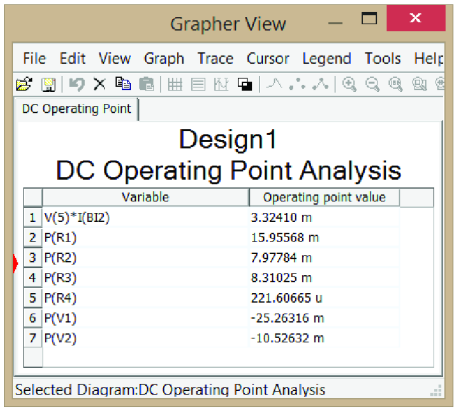
Figure 3.38 (a) Circuit with a switch, and (b) its Multisim representation.



(a) Multisim circuit of Fig. 3-32(a) ready for power calculations



(b) Selected variables for analysis visible in DC Operating Point Analysis window



(c) Output of simulations (remember that all values are in watts)

Figure 3.39 Multisim procedure for calculating power consumed (or generated) by the seven elements in the circuit of **Fig.** 3.37**(a)**.

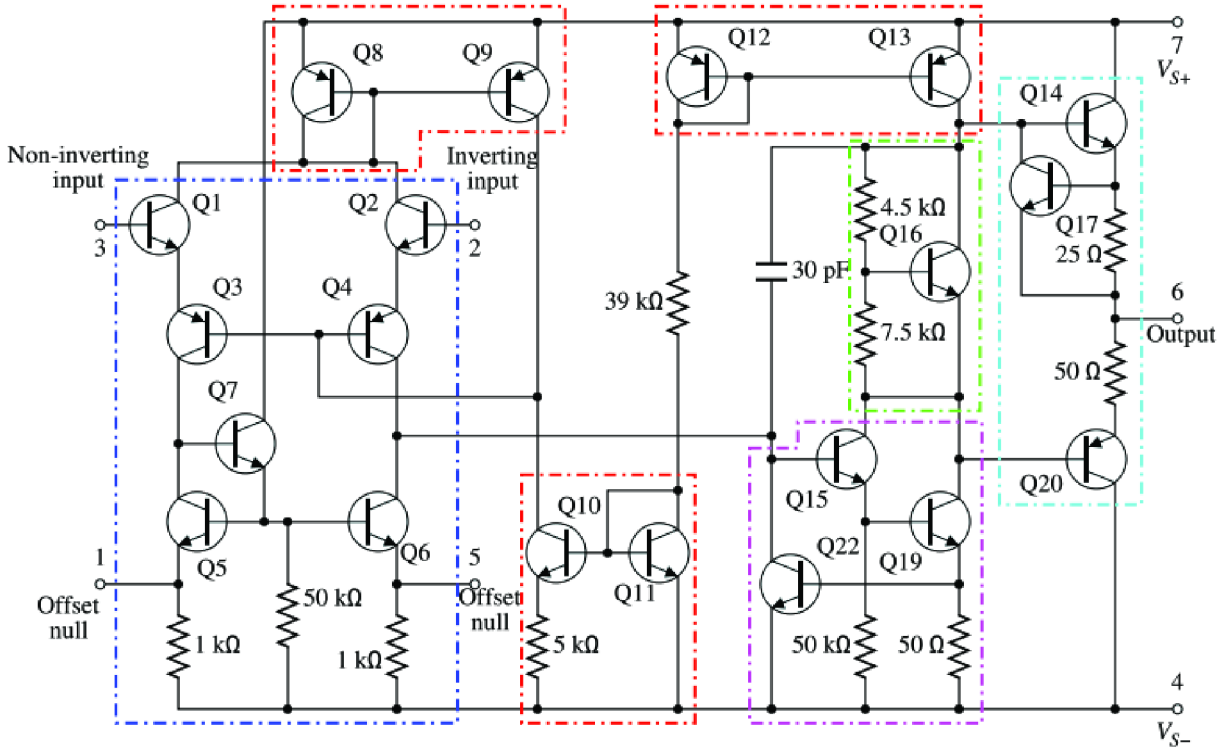


Figure 4.1 The circuit diagram of the Model 741 op amp consists of 20 transistors, several resistors, and one capacitor.

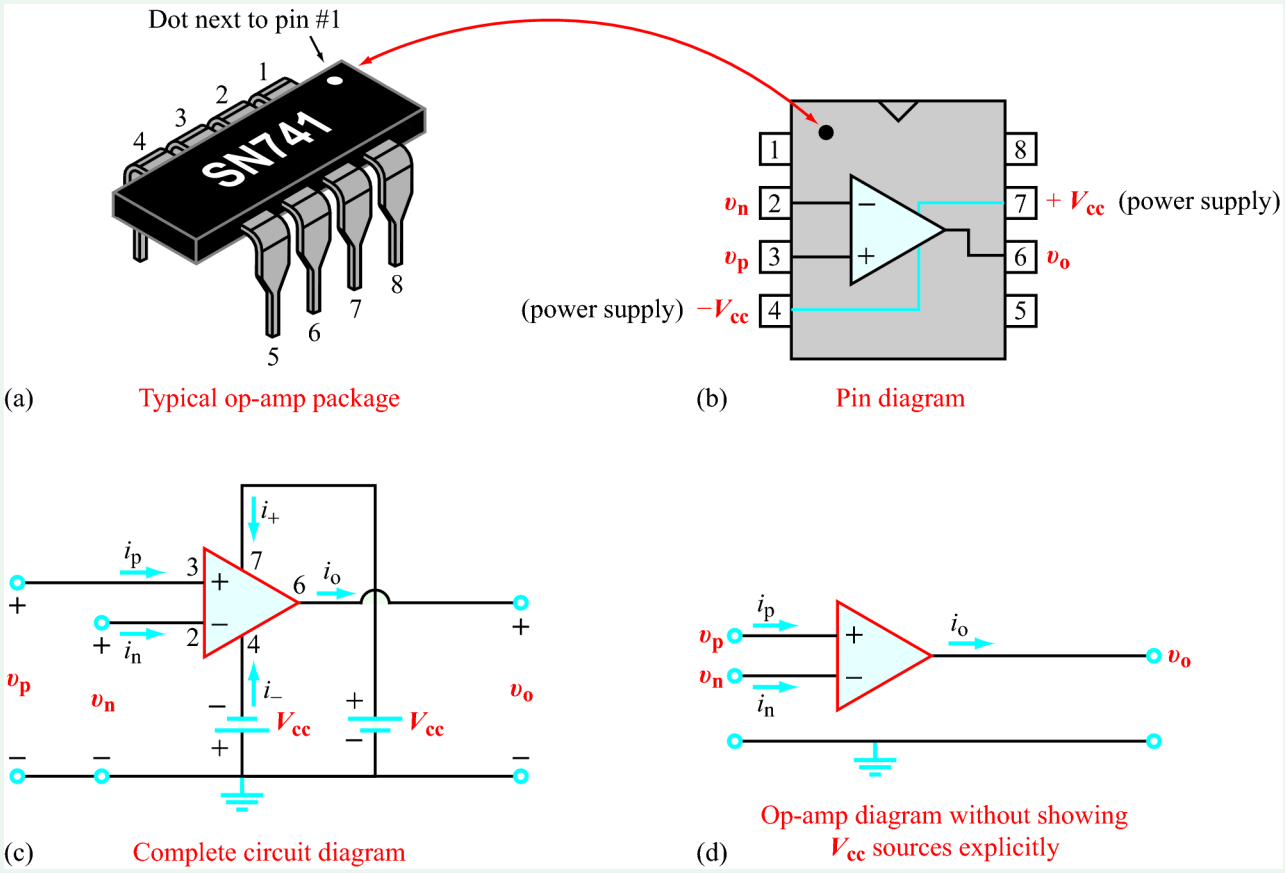


Figure 4.2 Operational amplifier.

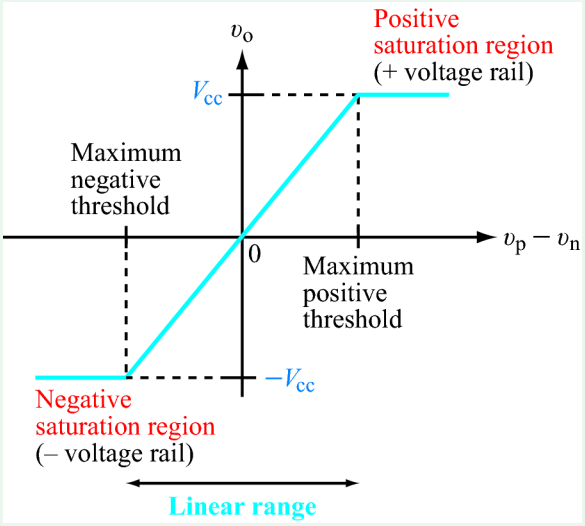


Figure 4.3 Op-amp transfer characteristics. The linear range extends between $v_o = -V_{cc}$ and $+V_{cc}$. The slope of the line is the op-amp gain A

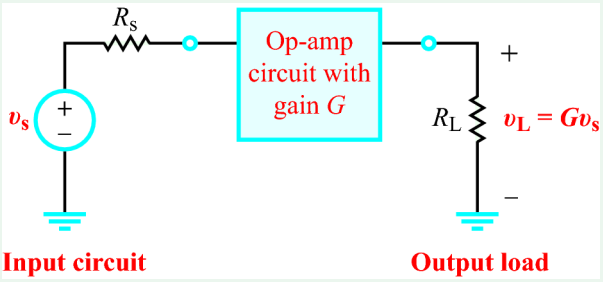


Figure 4.4 Circuit gain G is the ratio of the output voltage υ_L to the signal input voltage υ_s.

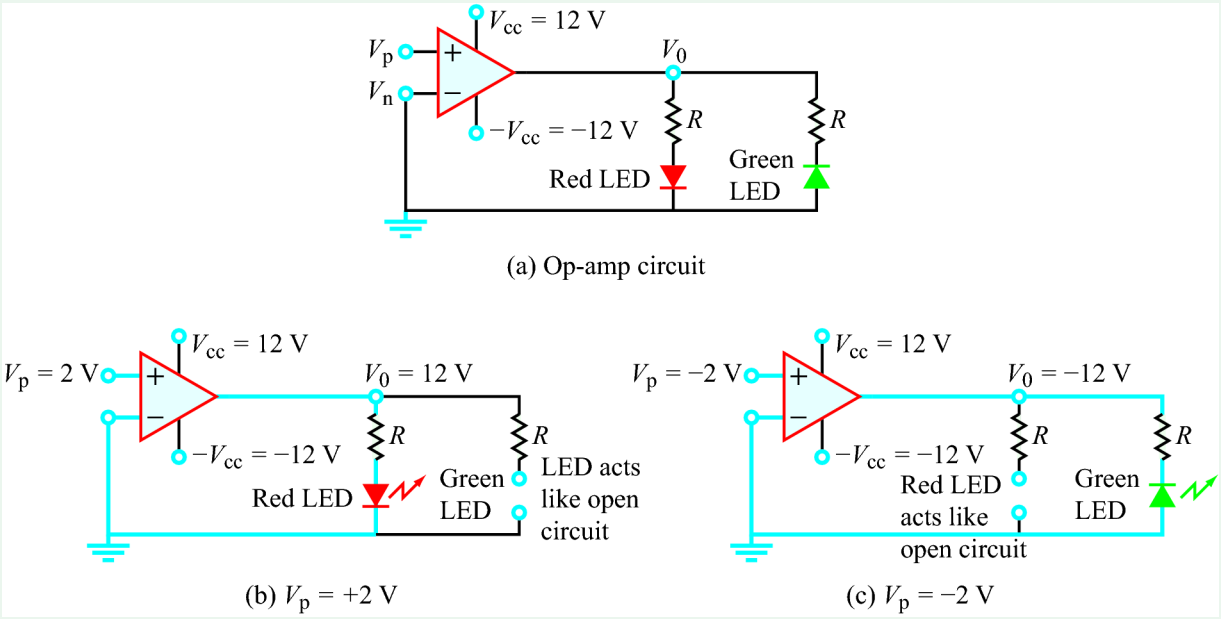


Figure 4.5 Op amp operated as a switch. The $\pm V_{cc}$ flags indicate the dc supply voltages connected to pins 7 and 4.

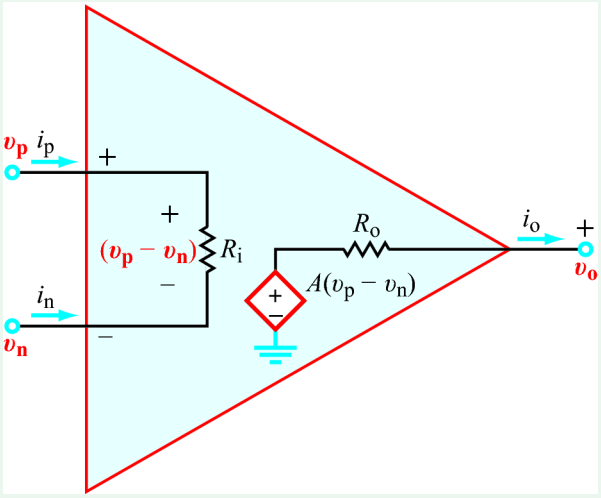


Figure 4.6 Equivalent circuit model for an op amp operating in the linear range ($v_o \leq |V_{cc}|$). Voltages v_p, v_n, and v_o are referenced to ground.

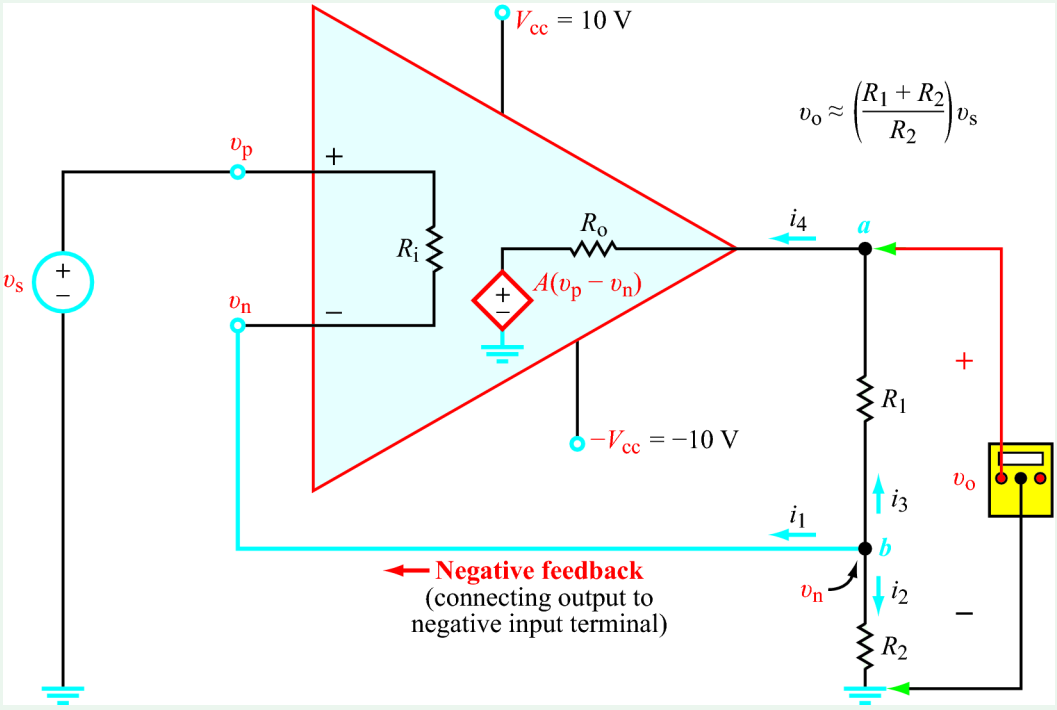


Figure 4.7 Noninverting amplifier circuit of Example 4-1.

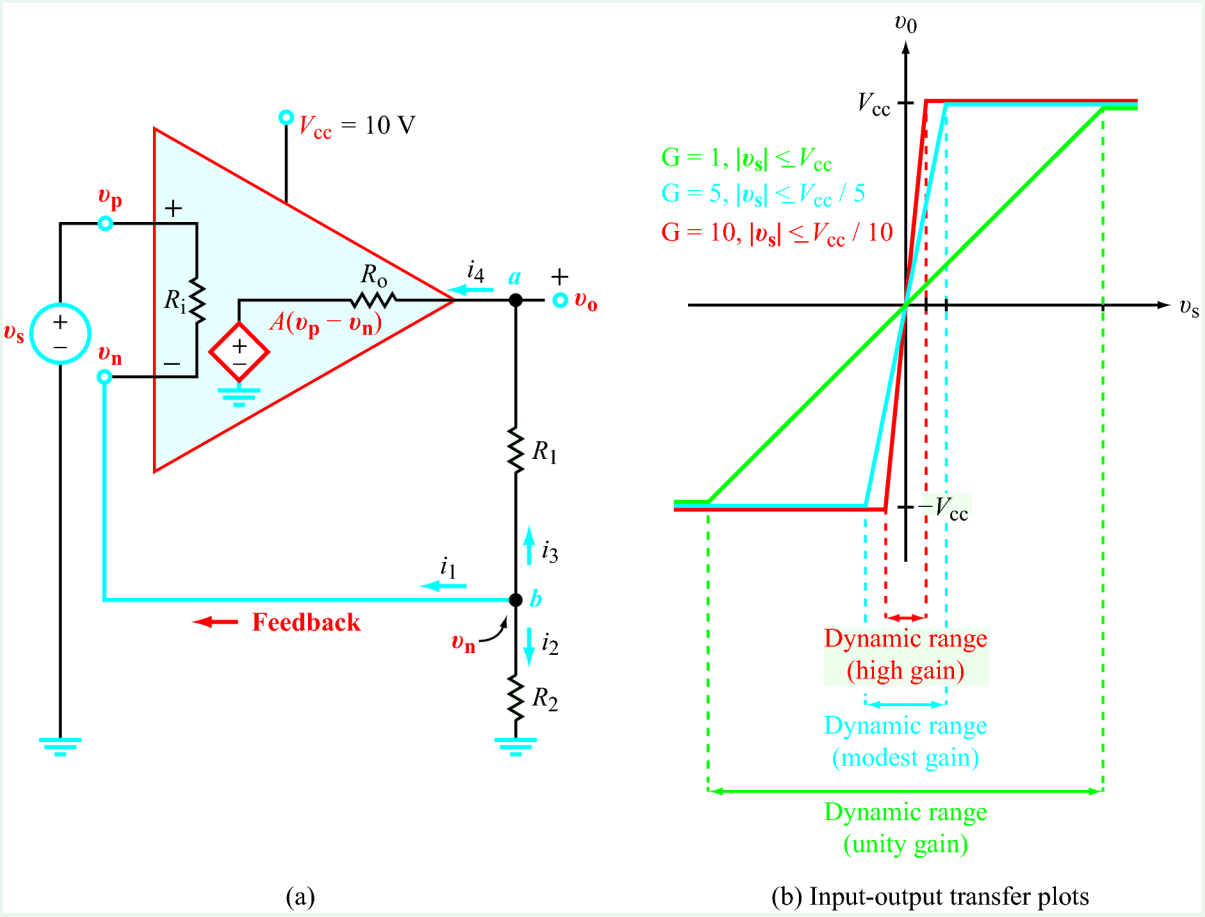


Figure 4.8 Trade-off between gain and dynamic range.

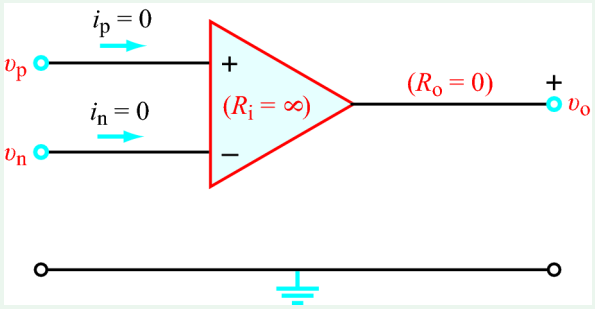


Figure 4.9 Ideal op-amp model.

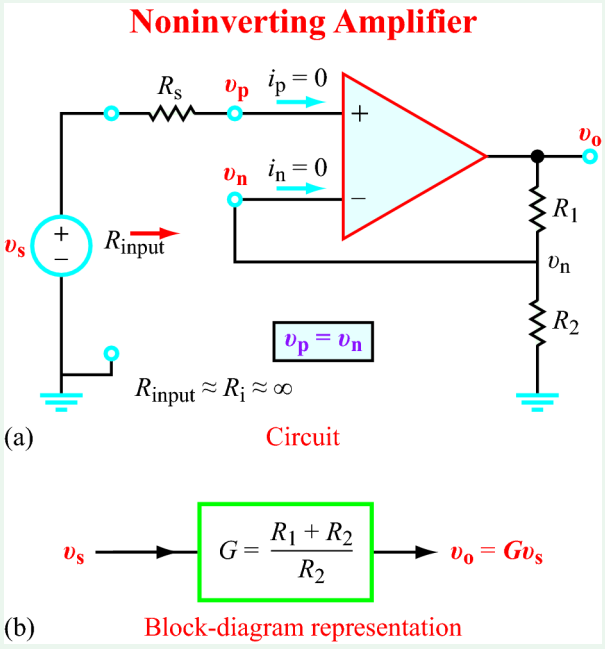


Figure 4.10 Noninverting amplifier circuit: (a) using ideal op-amp model and (b) equivalent block-diagram representation.

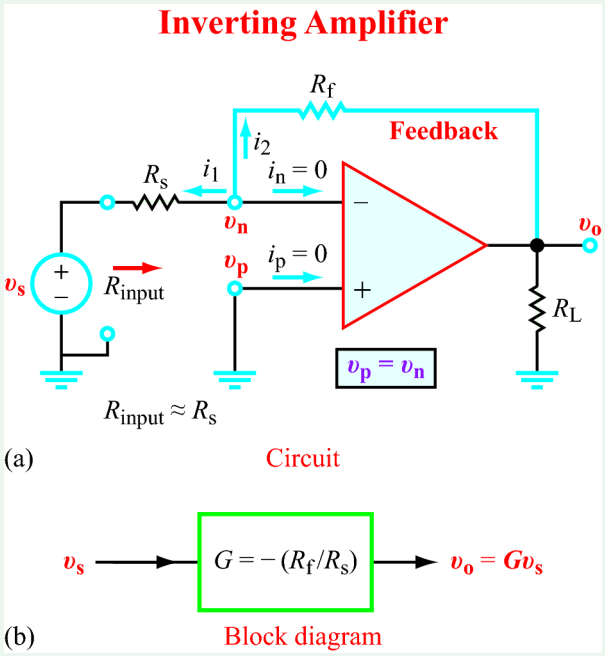


Figure 4.11 Inverting amplifier circuit and its block-diagram equivalent.

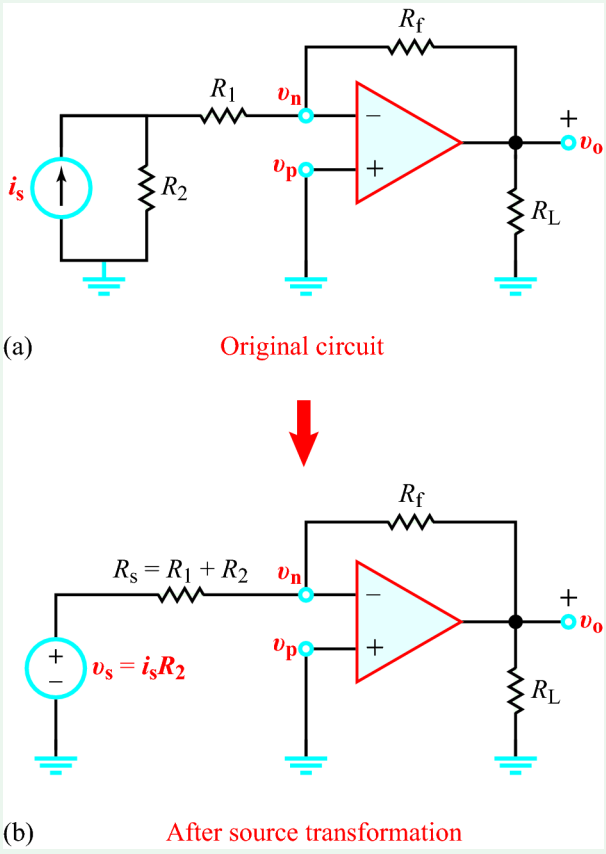


Figure 4.12 Inverting amplifier circuit of Example 4-2.

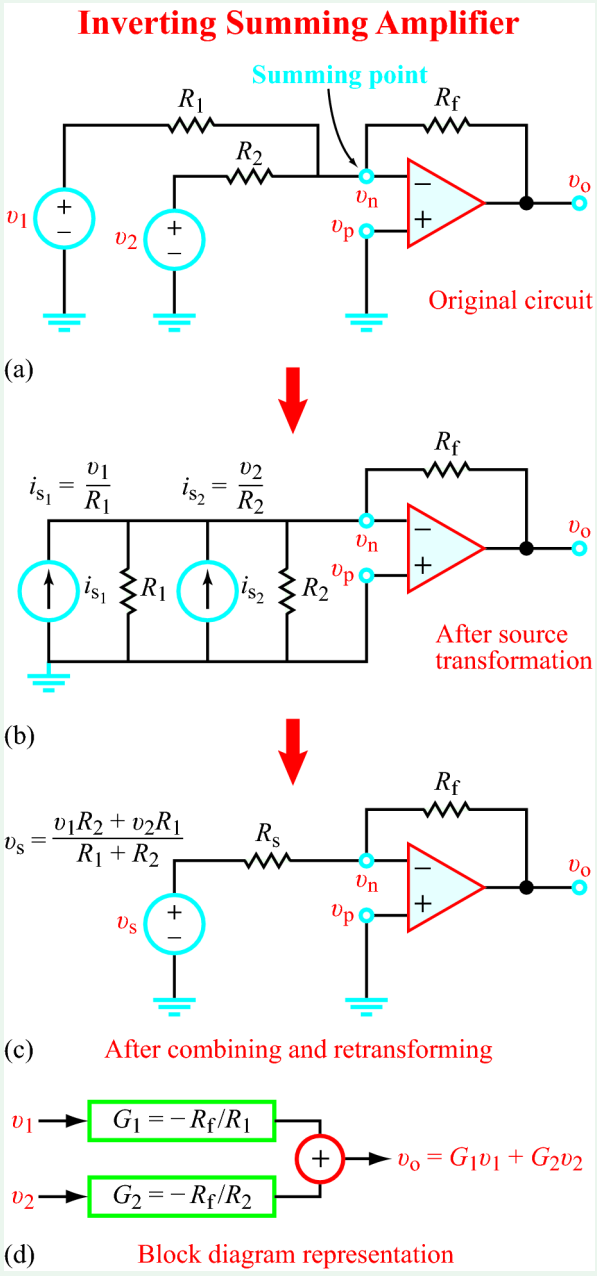
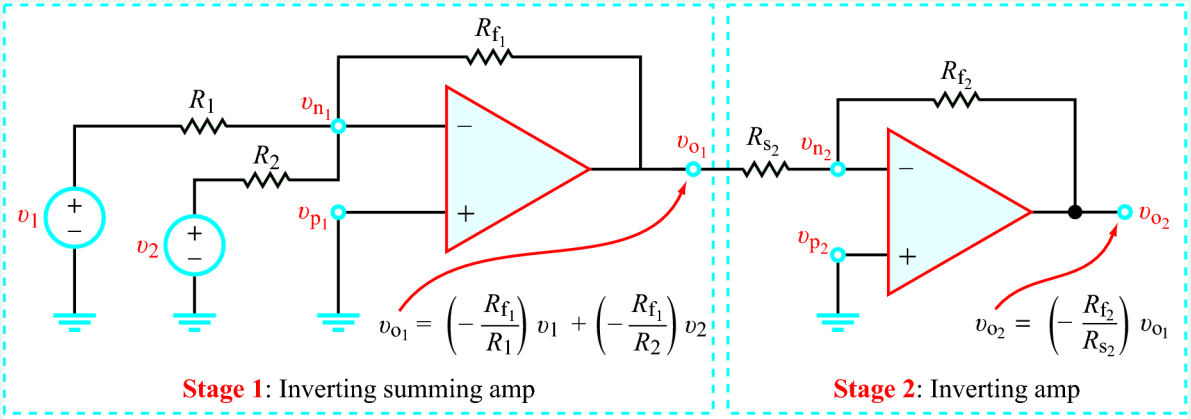
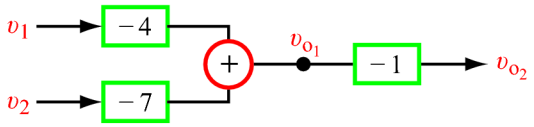


Figure 4.13 Inverting summing amplifier.



(a) Two-stage circuit

Circuit Design	
R_1	14 kΩ
R_2	8 kΩ
R_{f_1}	56 kΩ
R_{s_1}	20 kΩ
R_{f_2}	20 kΩ



(b) Block diagram

Figure 4.14 Two-stage circuit realization of $v_o = 4v_1 + 7v_2$.

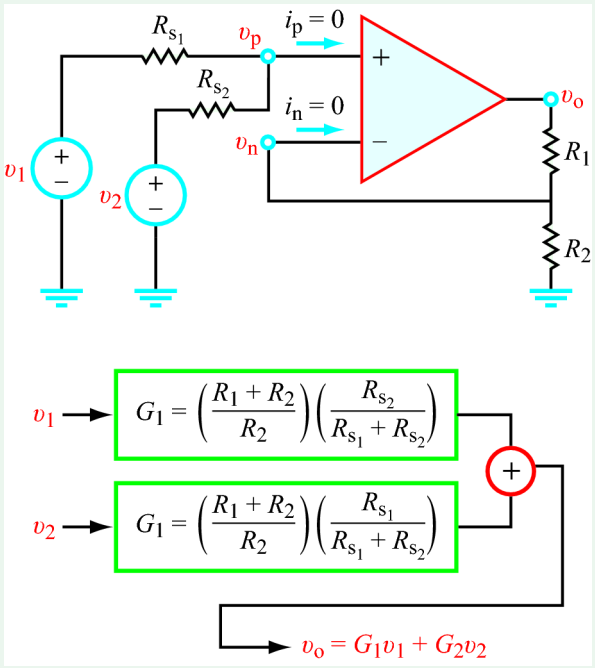
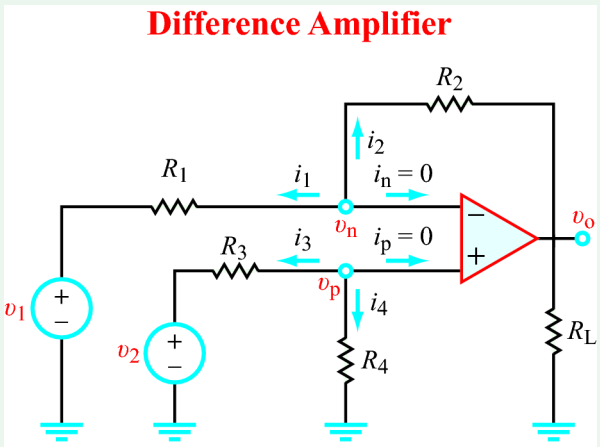
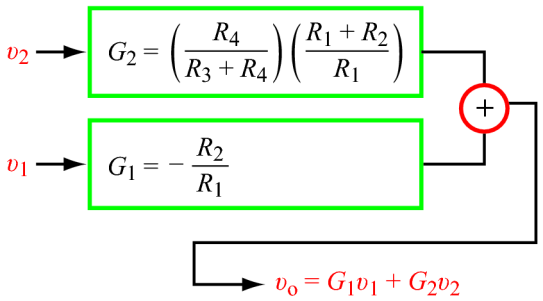


Figure 4.15 Noninverting summer.

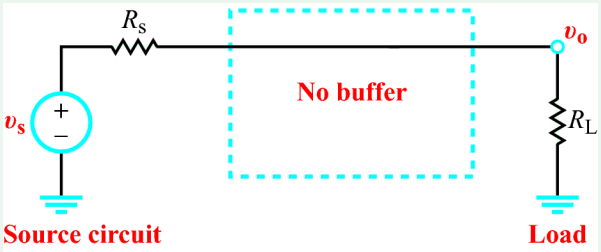


(a) Difference circuit

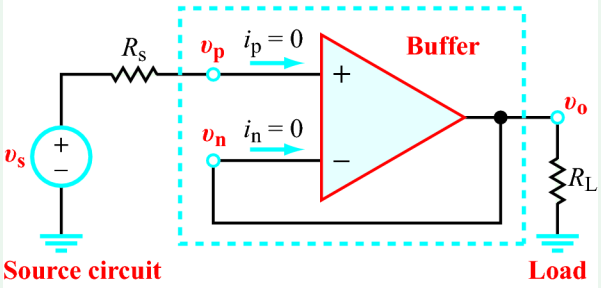


(b) Block diagram

Figure 4.16 Difference-amplifier circuit.



(a) Source circuit connected directly to a load



(b) Source circuit separated by a buffer

Figure 4.17 The voltage follower provides no voltage gain ($v_o = v_s$), but it insulates the input circuit from the load.

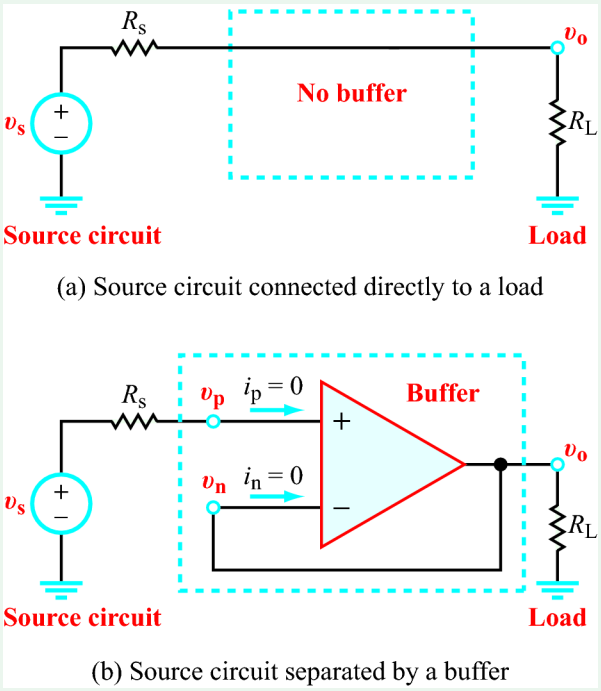


Figure 4.18 Block-diagram representation (Example 4-4).

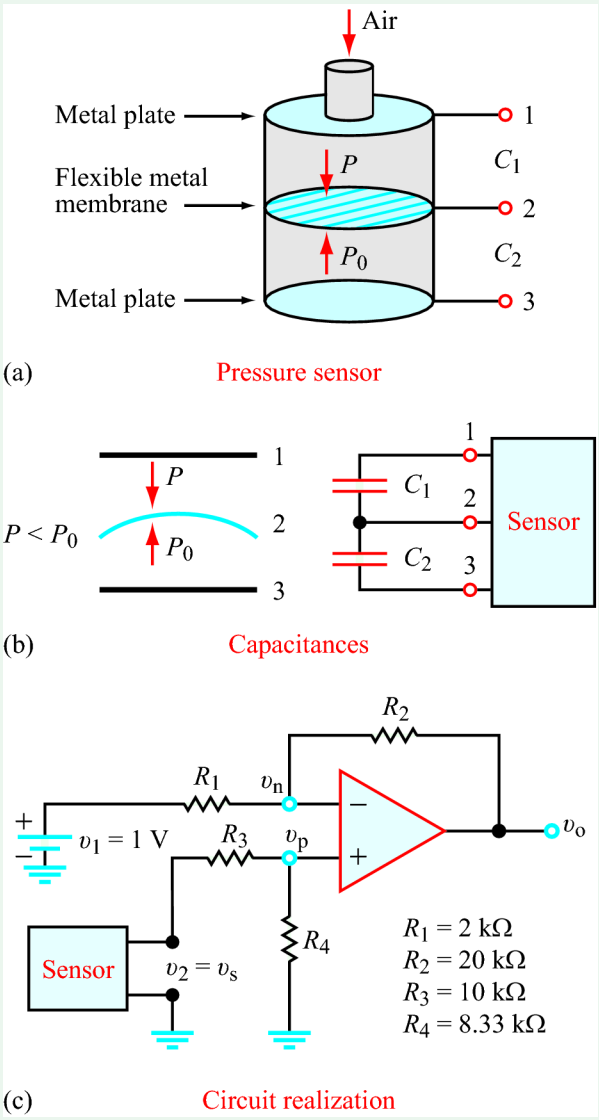


Figure 4.19 Design of a circuit for the pressure sensor of Example 4-5 with P_0 = pressure at sea level and P = pressure at height h.

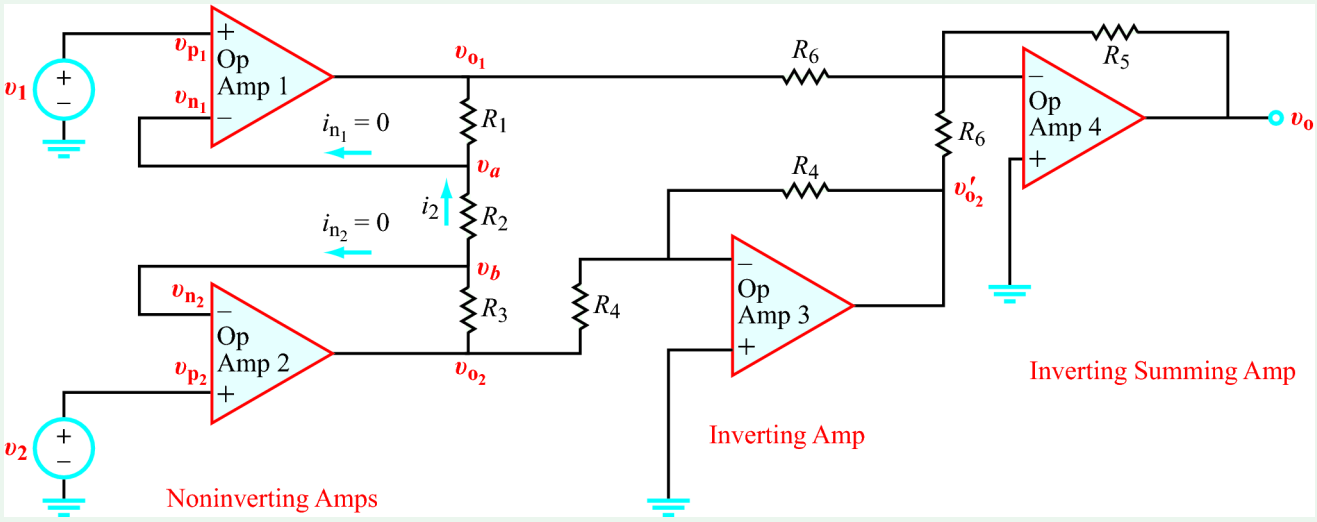


Figure 4.20 Example 4-6.

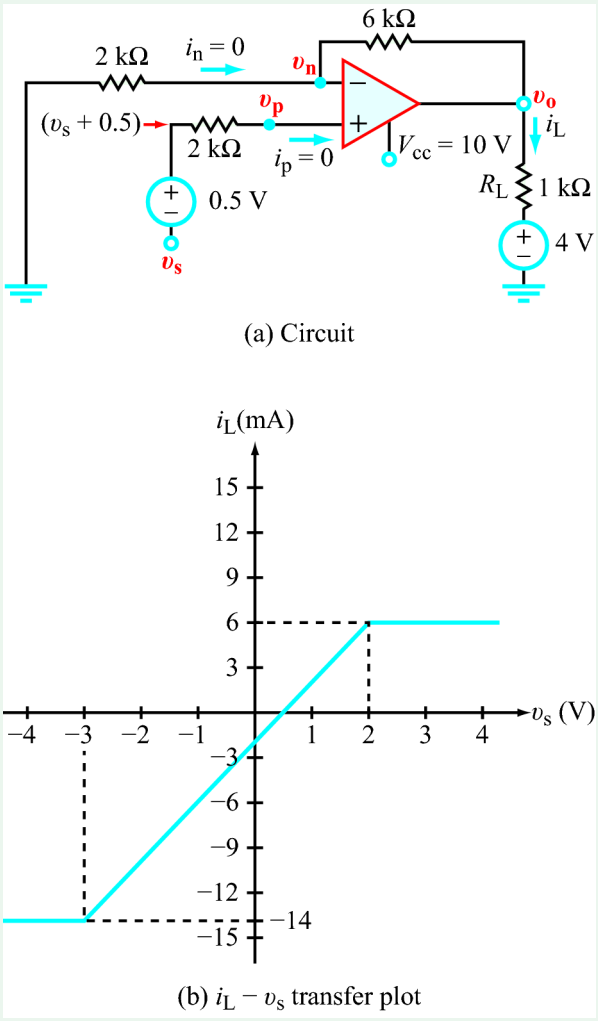


Figure 4.21 Circuit for Example 4-7.

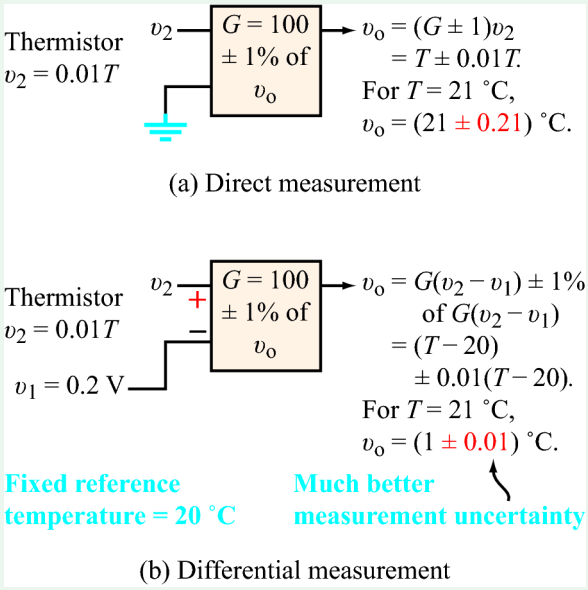


Figure 4.22 Comparison of direct and differential measurement uncertainties.

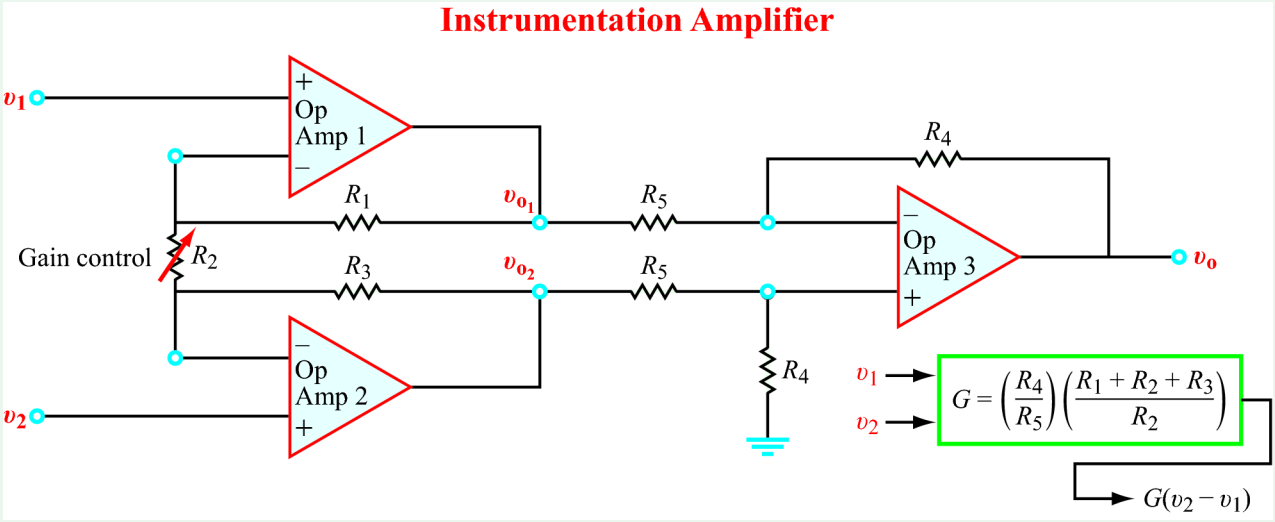


Figure 4.23 Instrumentation-amplifier circuit.

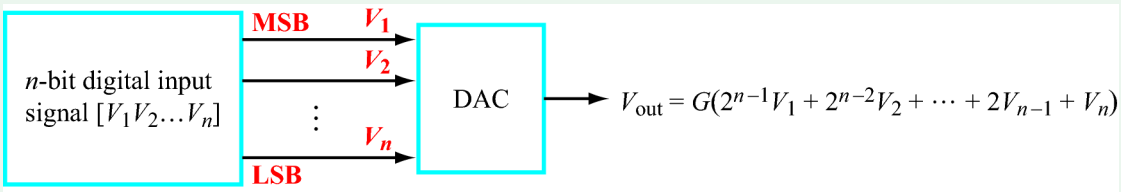


Figure 4.24 A digital-to-analog converter transforms a digital signal into an analog voltage proportional to the decimal value of the digital sequence.

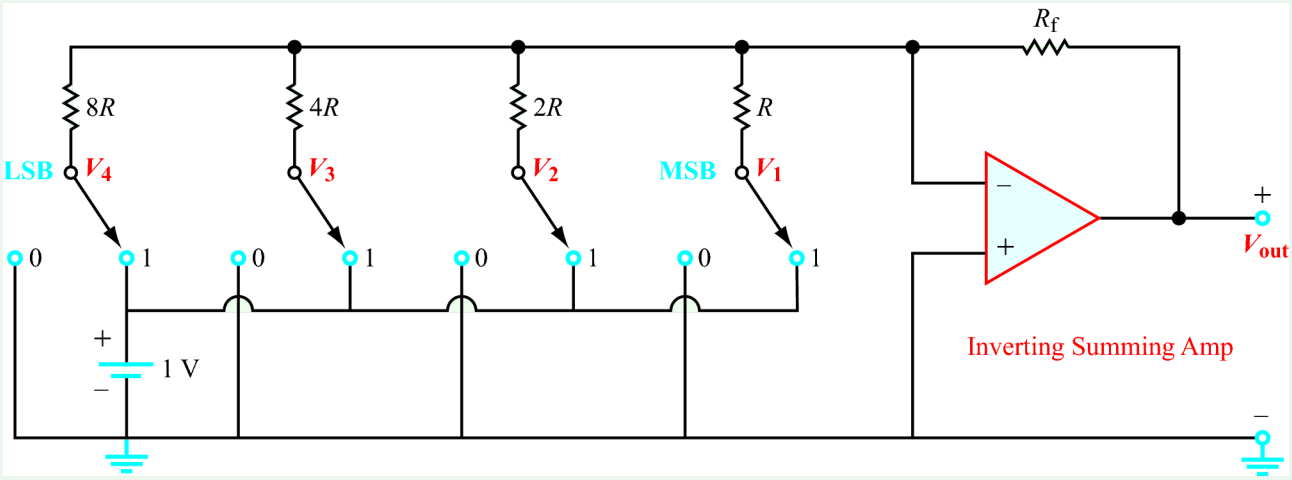
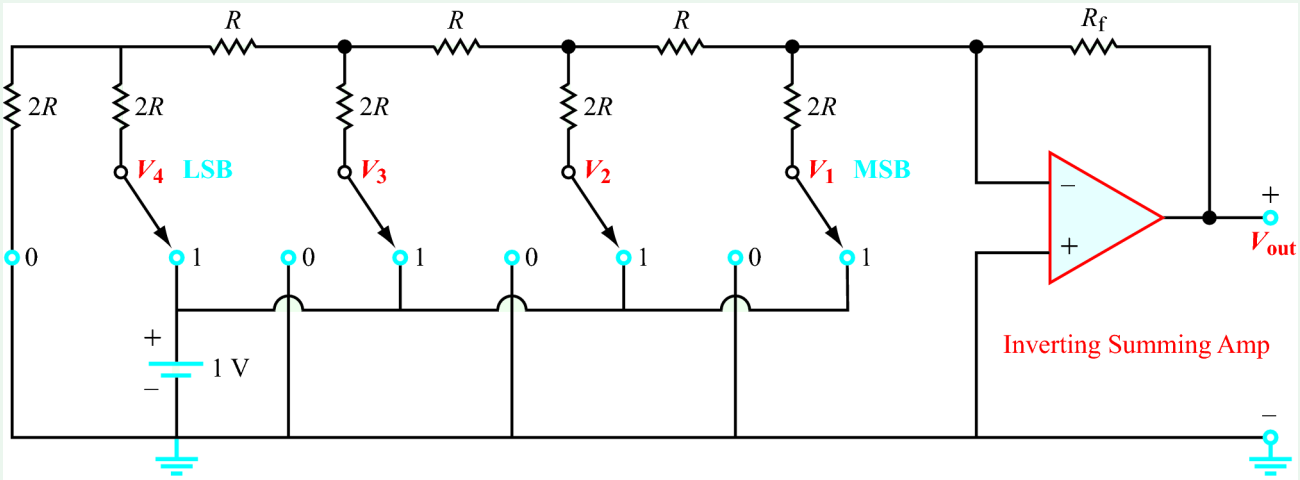
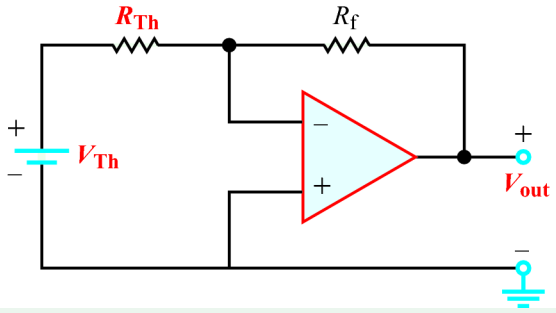


Figure 4.25 Circuit implementation of a DAC.



(a) R–$2R$ ladder network

(b) Thévenin equivalent circuit



$$V_{Th} = \frac{V_1}{2} + \frac{V_2}{4} + \frac{V_3}{8} + \frac{V_4}{16}$$

$$R_{Th} = R$$

Figure 4.26 R–$2R$ ladder digital-to-analog converter.

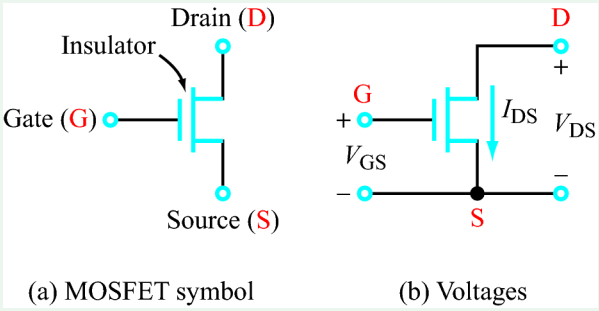


Figure 4.27 MOSFET symbol and voltage designations.

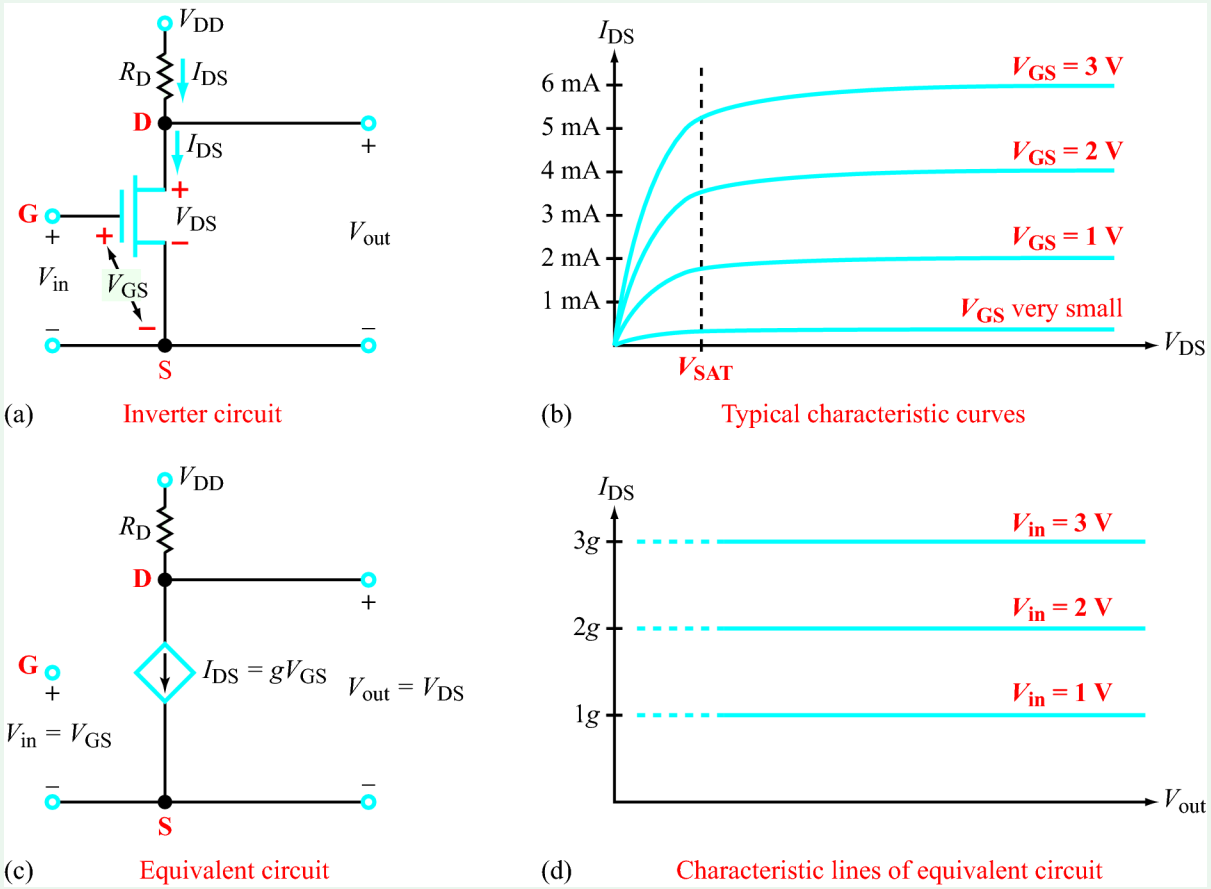


Figure 4.28 MOSFET (a) circuit, (b) characteristic curves, (c) equivalent circuit, and (d) associated characteristic lines.

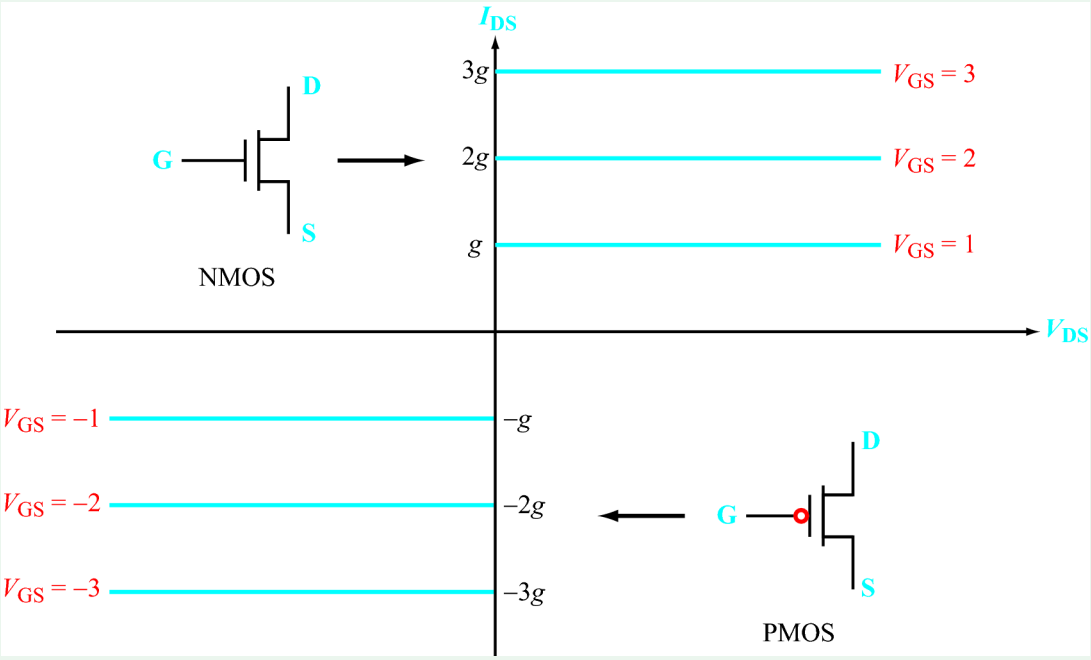


Figure 4.29 Complementary characteristic curves for NMOS and PMOS.

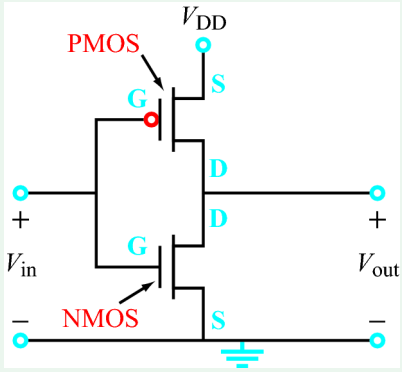
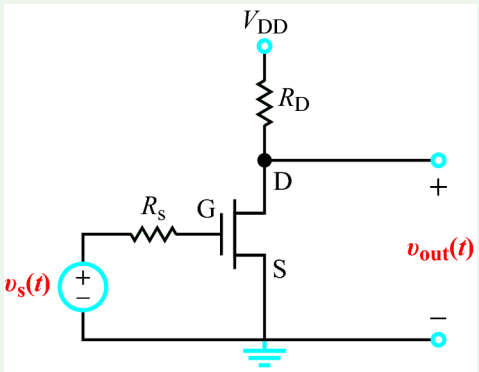
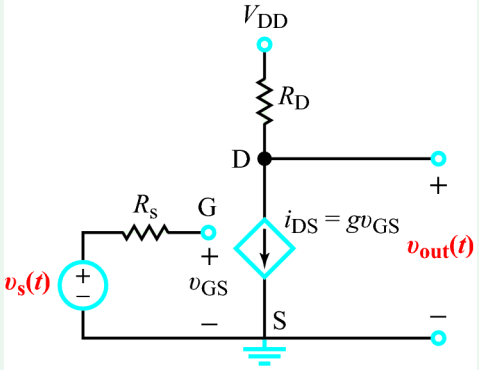


Figure 4.30 CMOS inverter.



(a) MOSFET amplifier



(b) Equivalent circuit

Figure 4.31 MOSFET amplifier circuit for Example 4-9.

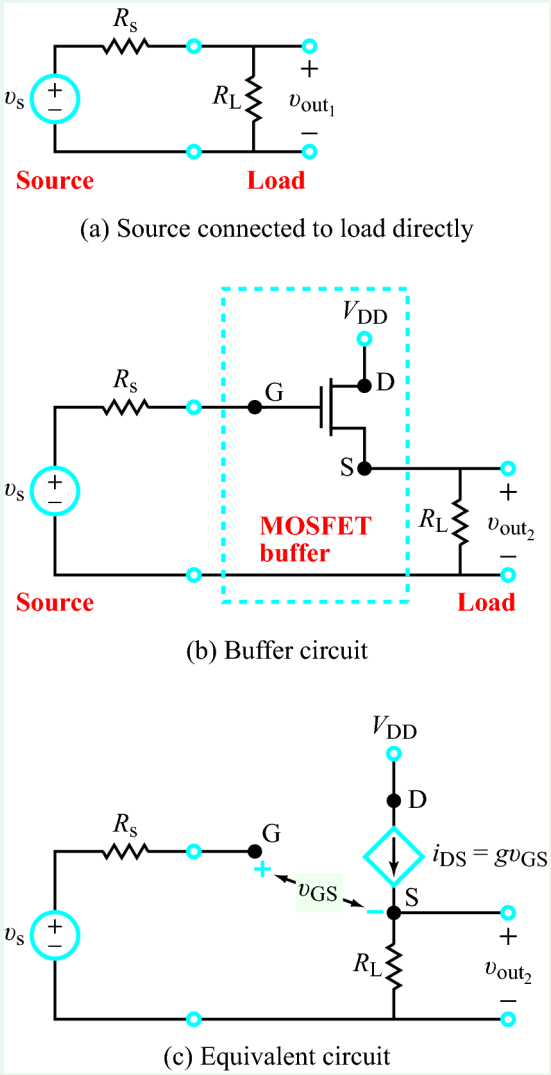


Figure 4.32 Buffer circuit for Example 4-10.

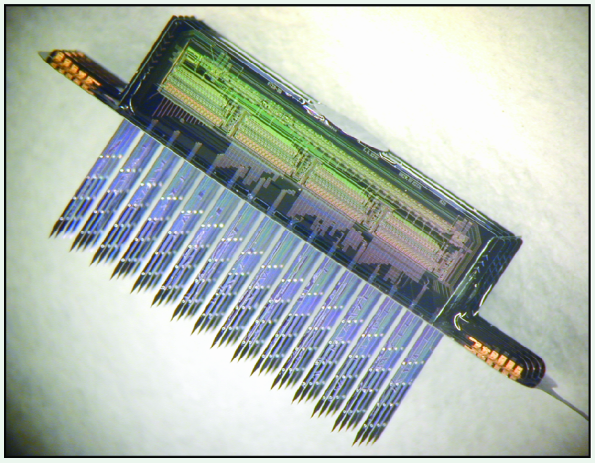


Figure 4.33 Three-dimensional neural probe (5 mm × 5 mm × 3 mm). (Courtesy of Prof. Ken Wise and Gayatri Perlin, University of Michigan.)

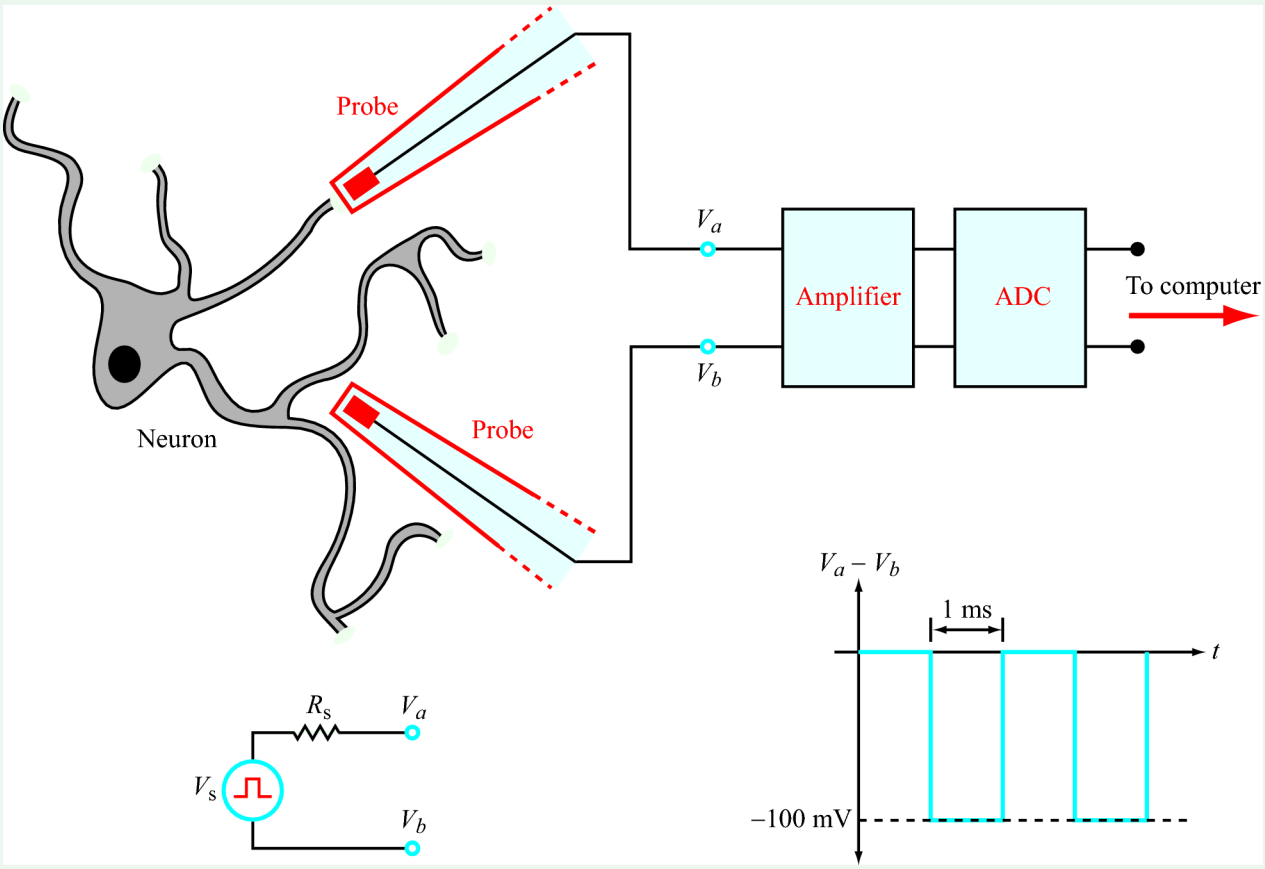


Figure 4.34 Neural-probe circuit for Example 4-11.

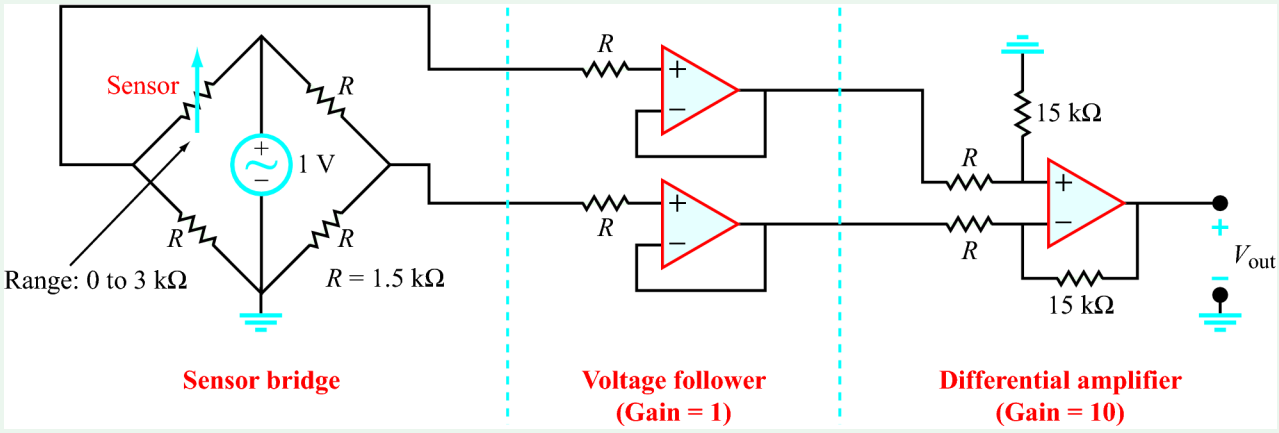


Figure 4.35 Wheatstone-bridge op-amp circuit.

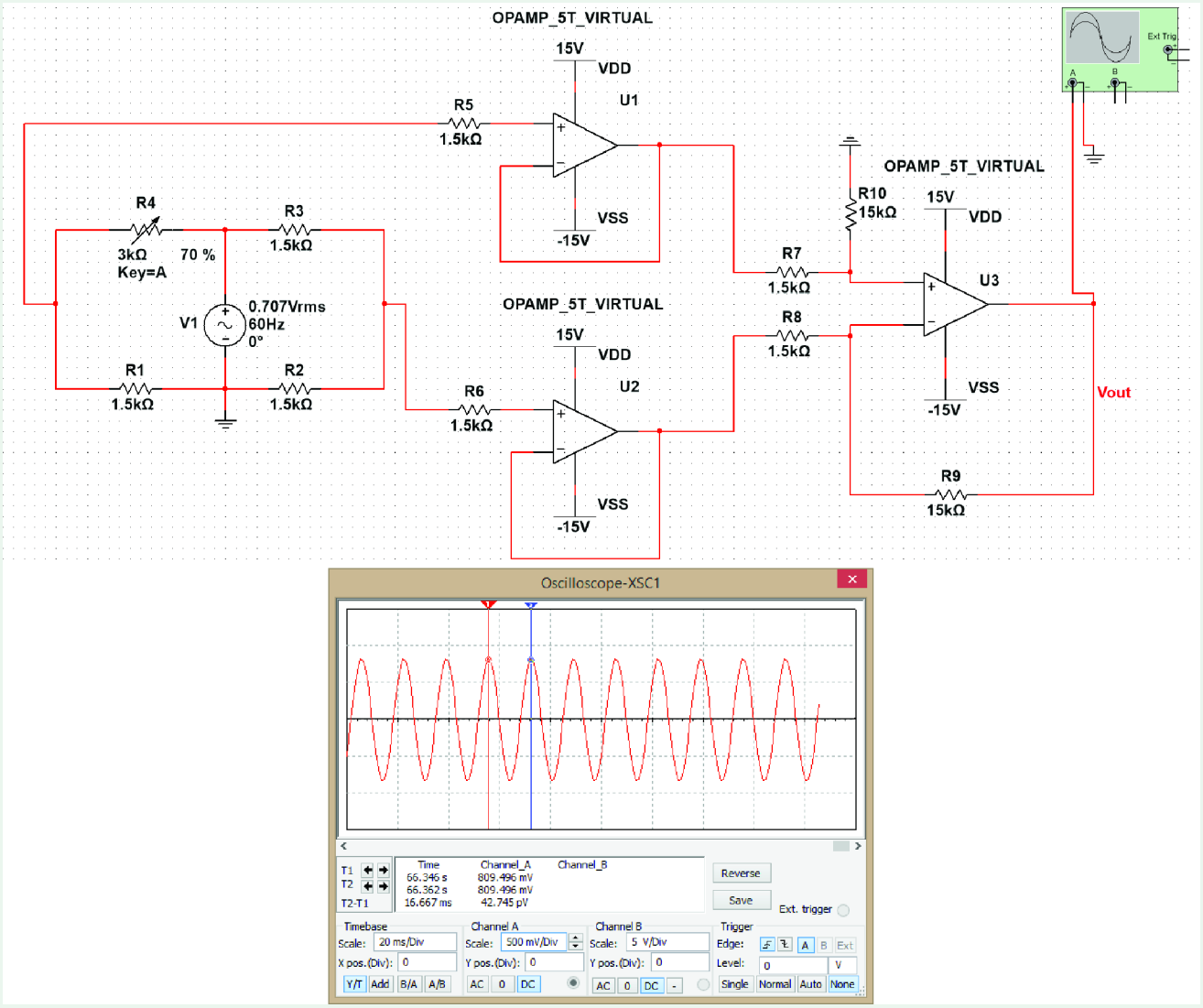


Figure 4.36 Multisim window of the circuit of **Fig.** 4.35. The oscilloscope trace shows the 60 Hz waveform of the output voltage. Had the voltage source been a dc source, the oscilloscope trace would have been a horizontal line.

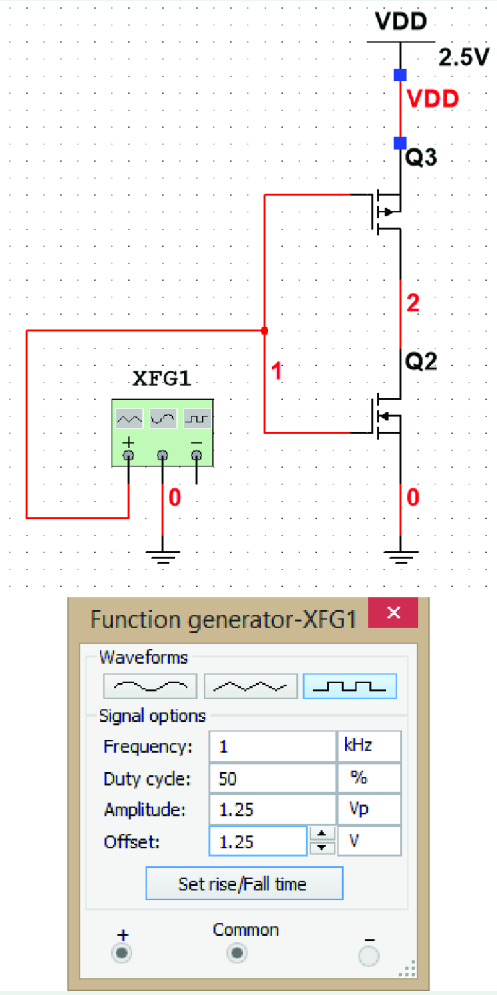
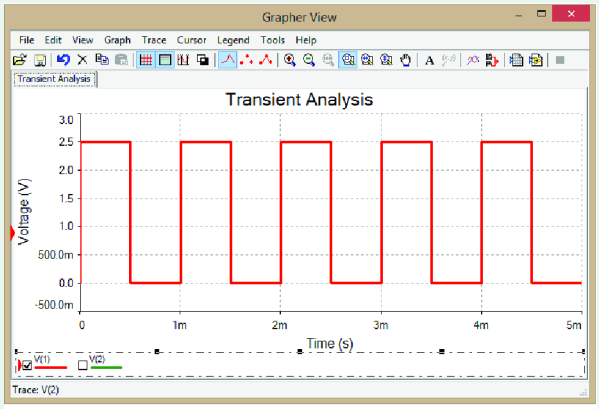
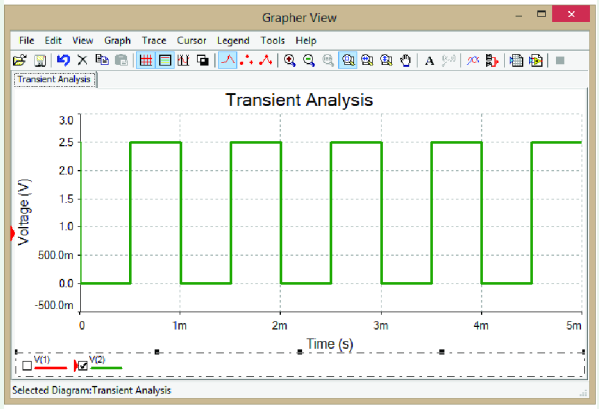


Figure 4.37 Multisim equivalent of the MOSFET circuit of **Fig.** 4.30.



(a) Input voltage



(b) Output voltage

Figure 4.38 Input and output voltages V(1) and V(2) in the circuit of **Fig.** 4.37 as a function of time.

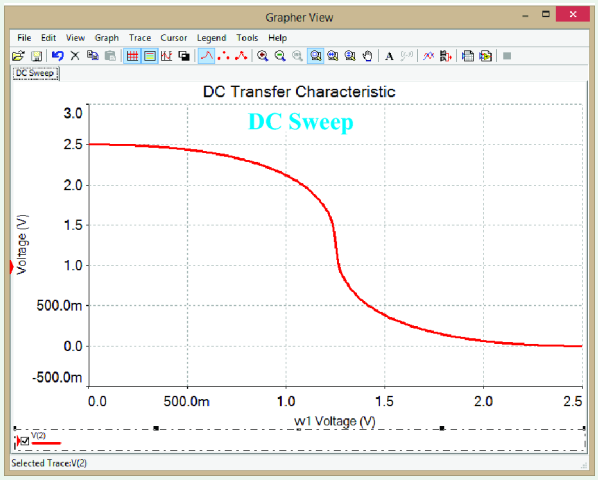


Figure 4.39 Output response of the MOSFET inverter circuit of **Fig.** 4.37 as a function of the amplitude of the input voltage.

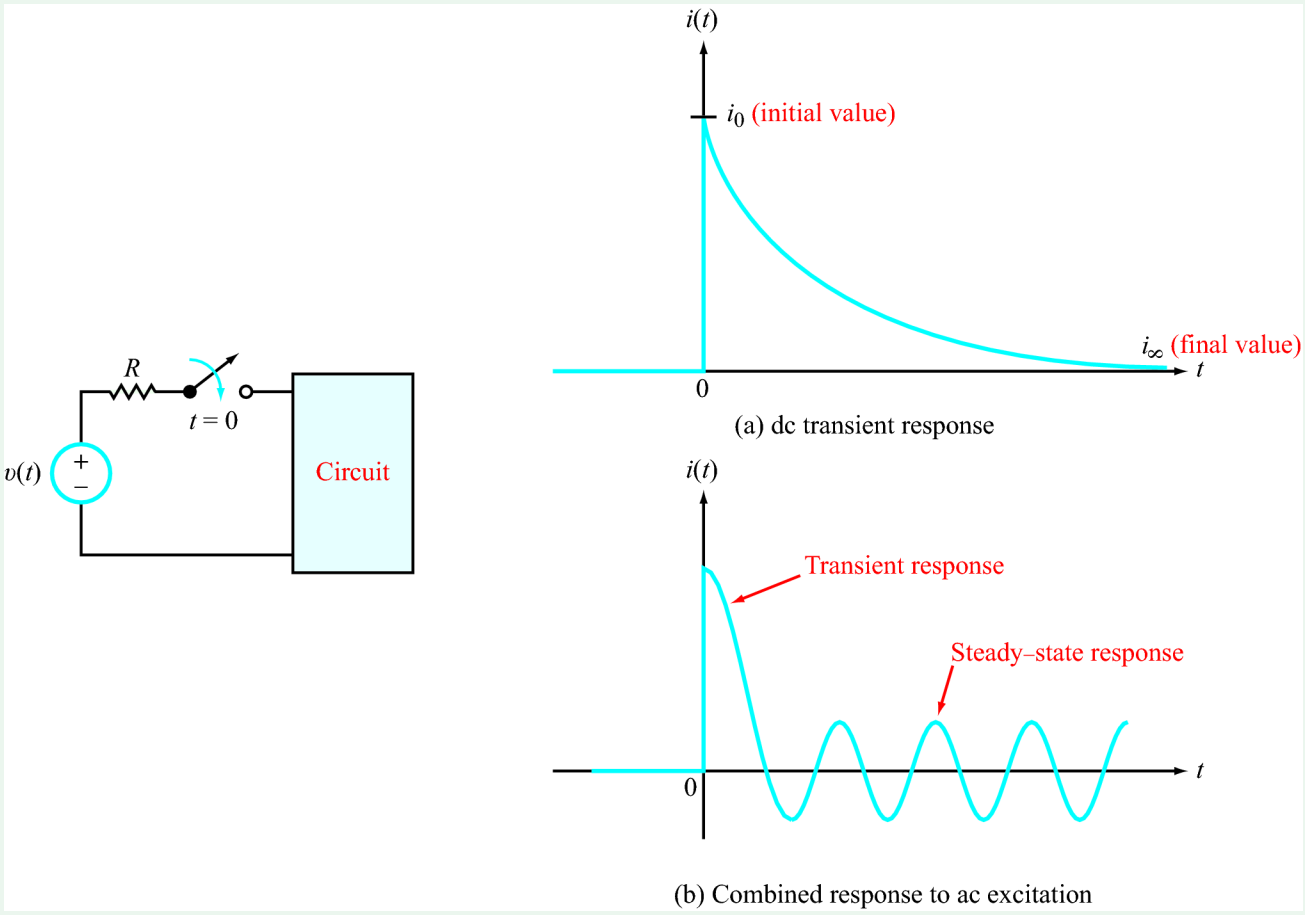


Figure 5.1 Circuit response to (a) dc source $\upsilon(t) = V_0$ and (b) ac source $\upsilon(t) = V_0 \cos \omega t$.

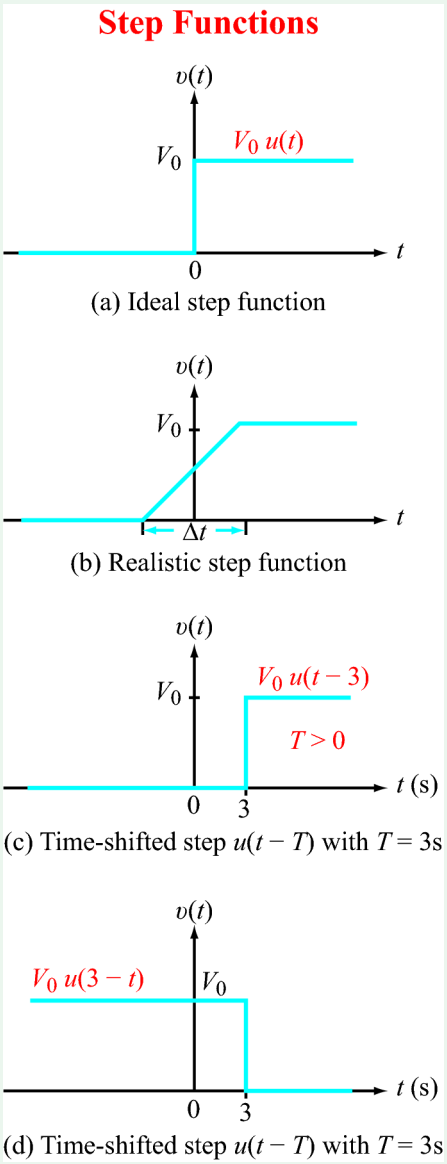


Figure 5.2 Step functions: (a) ideal step function, (b) realistic step function with transition duration Δt, (c) time-shifted step function $V_0\, u(t-3)$, (d) time-shifted step function $V_0\, u(3-t)$.

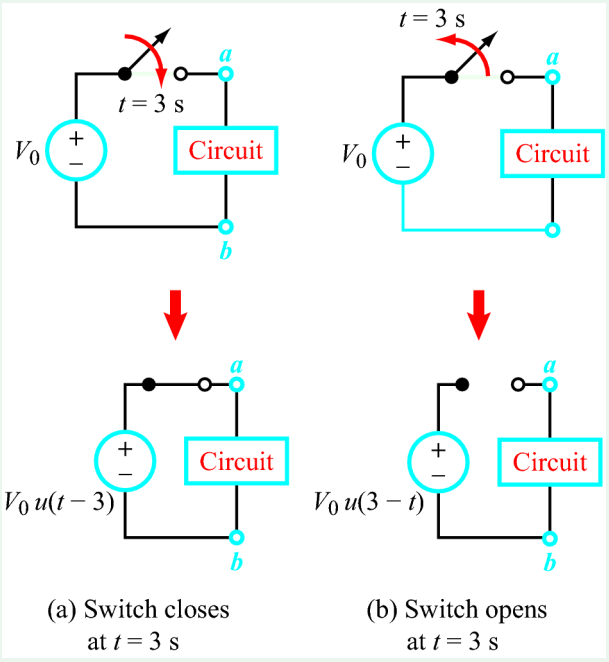


Figure 5.3 Connecting/disconnecting a voltage source to/from a circuit via a switch can be represented mathematically by a step function.

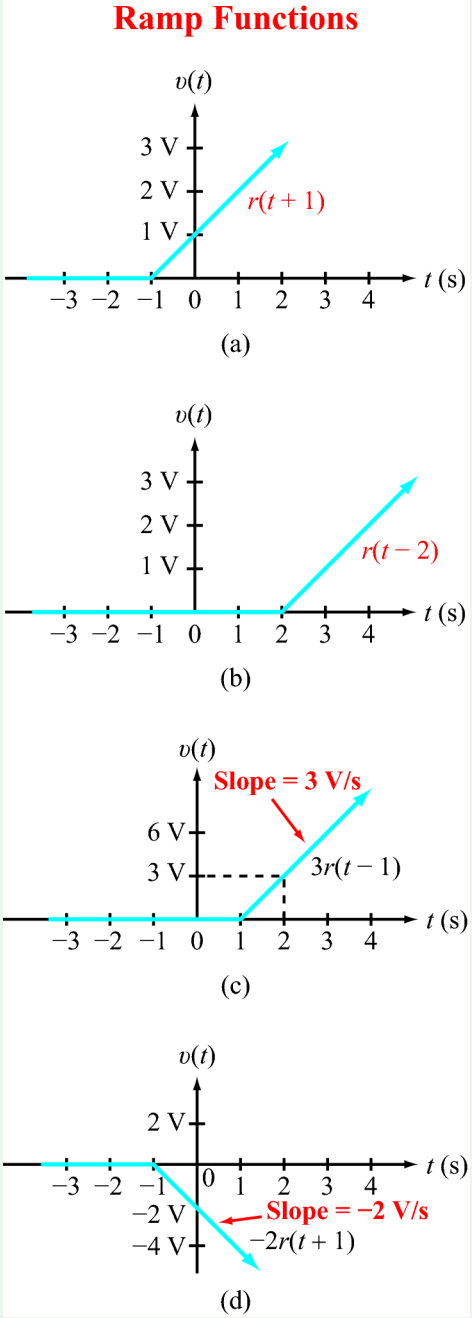


Figure 5.4 Time-shifted ramp functions.

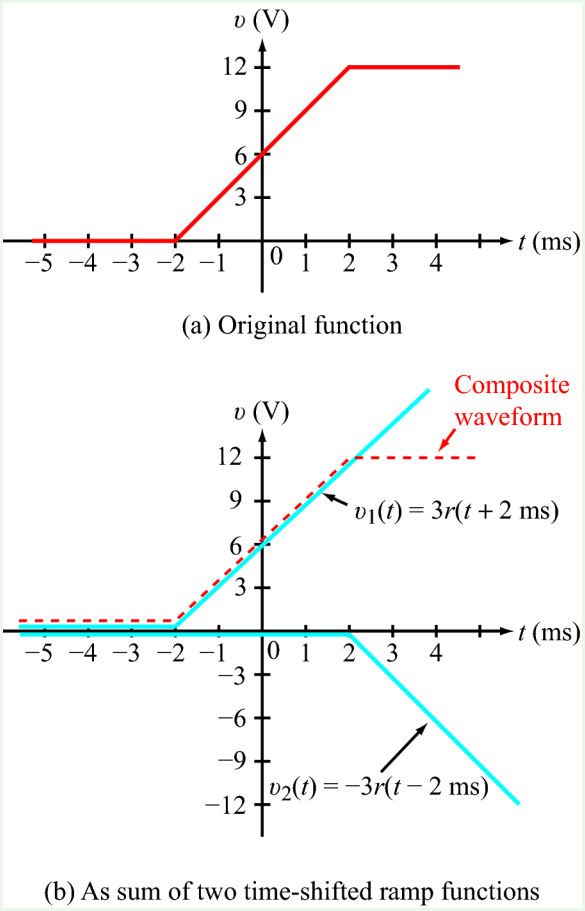
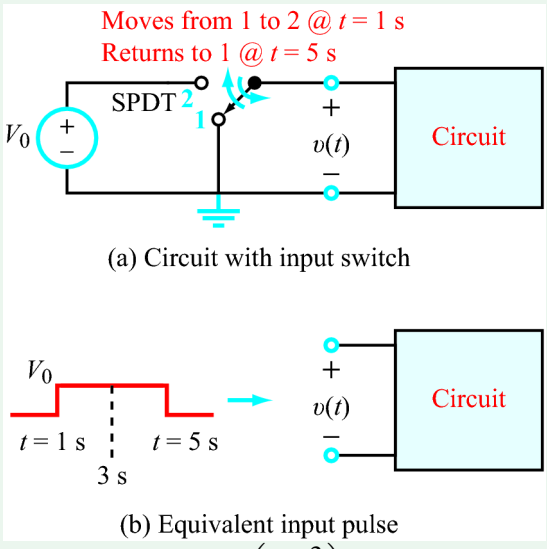


Figure 5.5 Step waveform of Example 5-1.



$$\text{rect}\left(\frac{t-3}{4}\right)$$

Figure 5.6 Connecting a switch to a dc source at $t = 1$ s and then returning it to ground at $t = 5$ s constitutes a voltage pulse centered at $T = 3$ s and of duration $\tau = 4$ s.

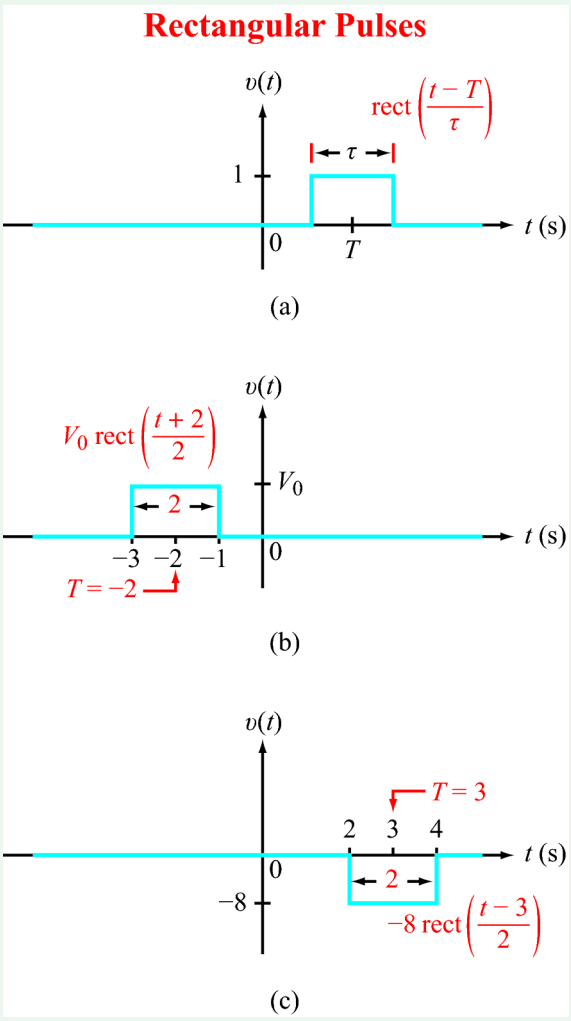


Figure 5.7 Rectangular pulses.

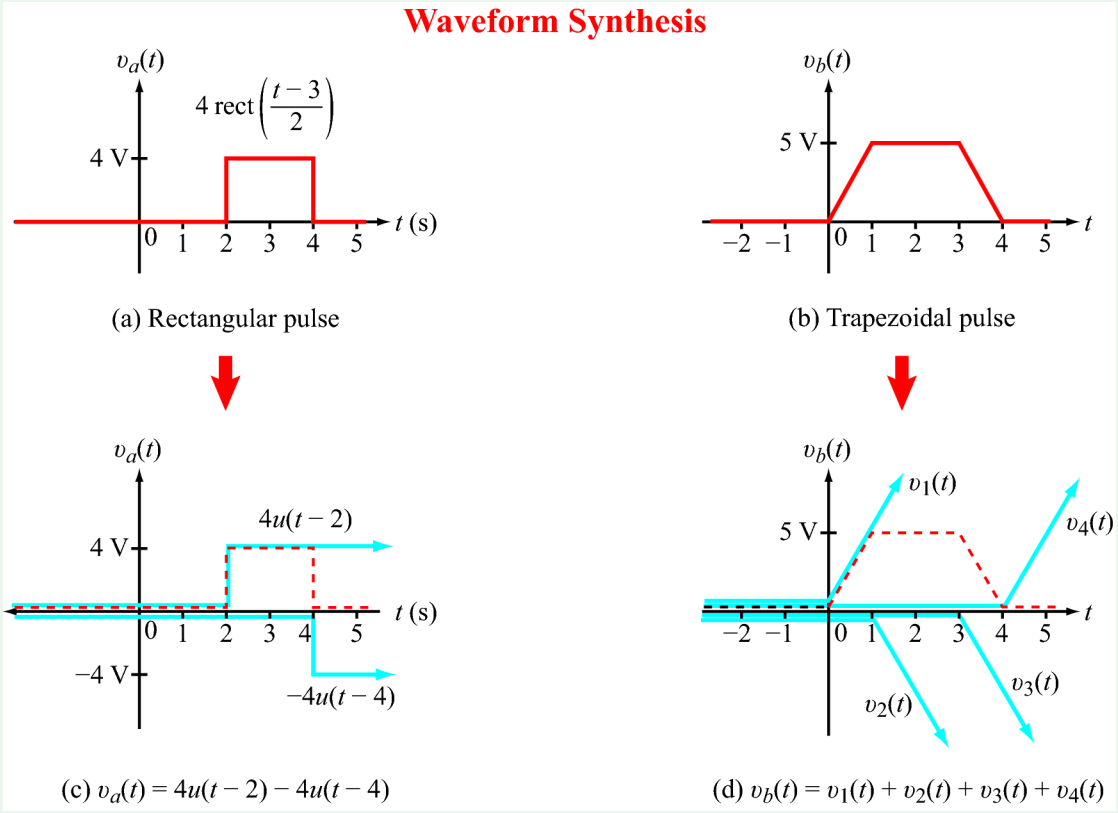


Figure 5.8 Rectangular and trapezoidal pulses of Example 5-2.

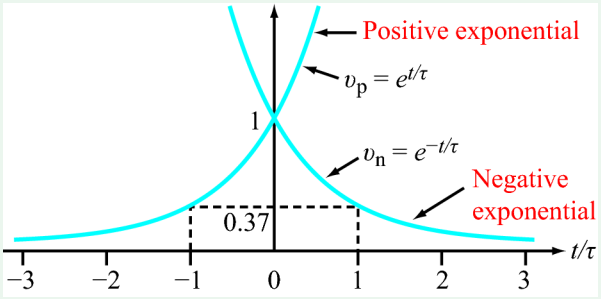


Figure 5.9 By $t = \tau$, the exponential function $e^{-t/\tau}$ has decayed to 37 percent of its original value at $t = 0$.

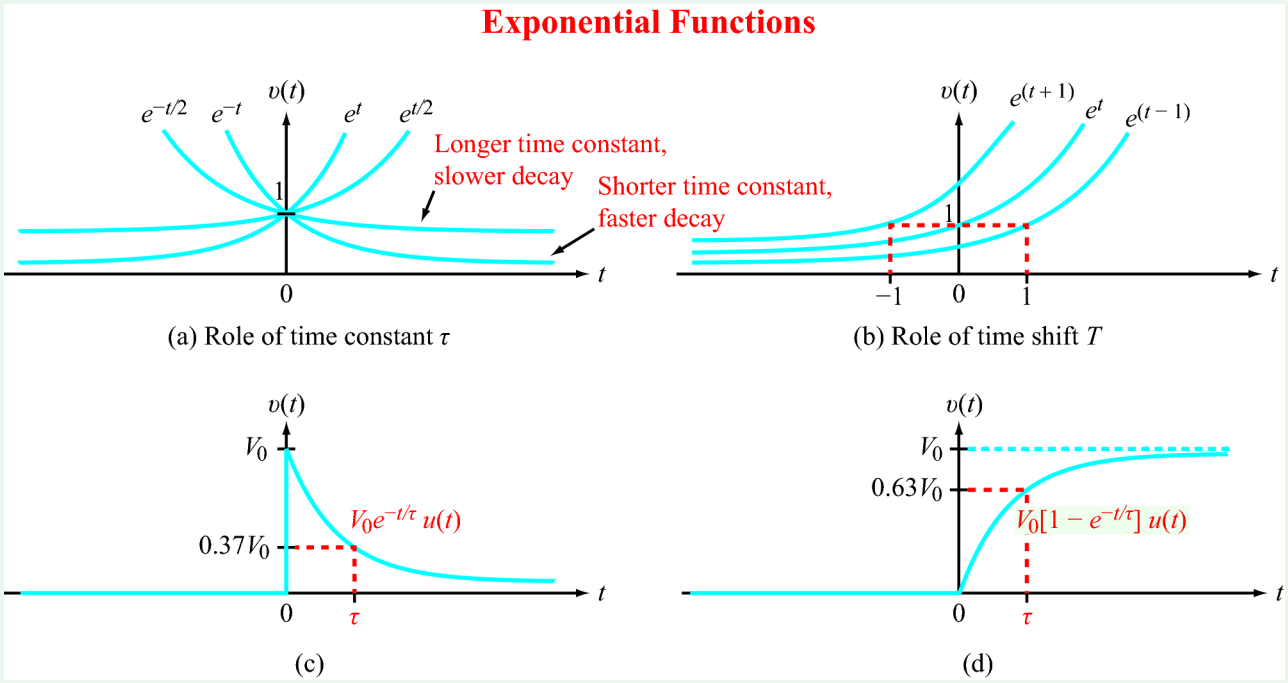


Figure 5.10 Properties of the exponential function.

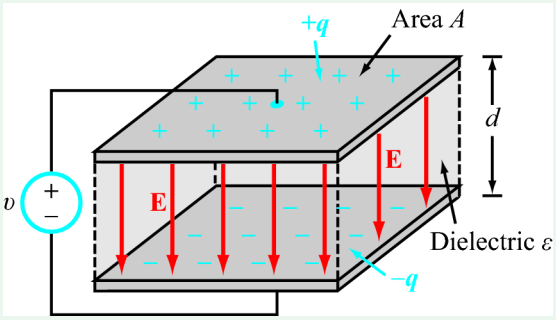
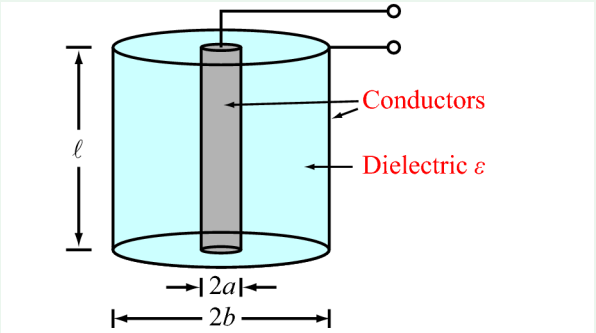
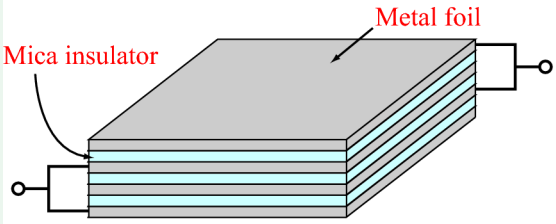


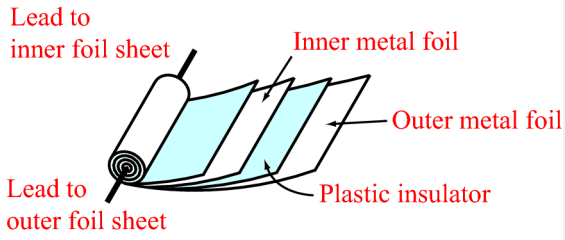
Figure 5.11 Parallel-plate capacitor with plates of area A, separated by a distance d, and filled with an insulating dielectric material of permittivity ε.



(a) Coaxial capacitor



(b) Mica capacitor



(c) Plastic foil capacitor

Figure 5.12 Various types of capacitors.

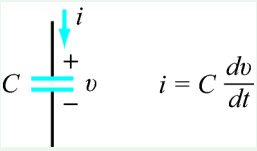


Figure 5.13 Passive sign convention for capacitor: if current i is entering the $(+)$ voltage terminal across the capacitor, then power is getting transferred into the capacitor. Conversely, if i is leaving the $(+)$ terminal, then power is getting released from the capacitor.

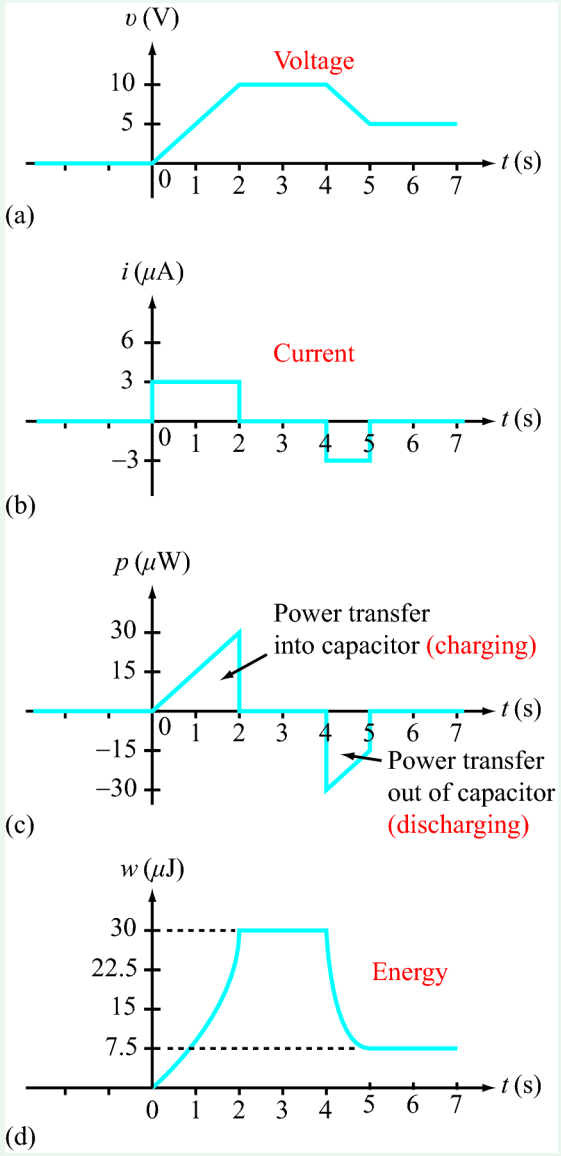


Figure 5.14 Example 5-3 waveforms for i, υ, p, and w.

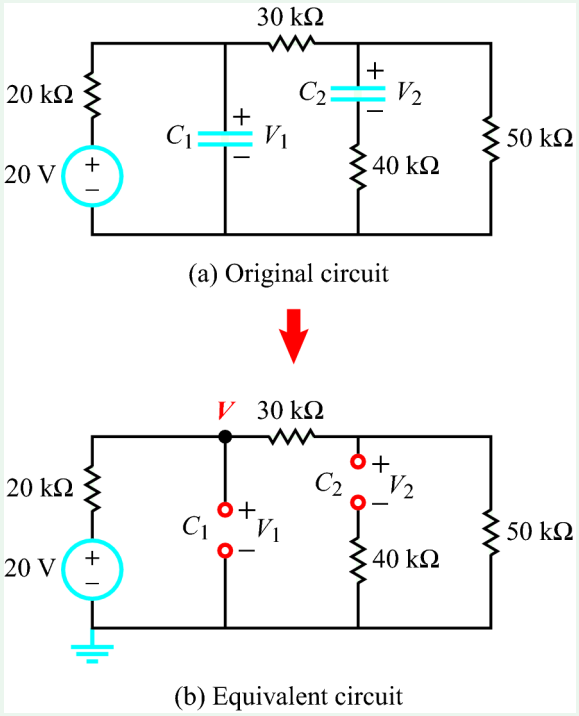


Figure 5.15 Under dc conditions, capacitors behave like open circuits.

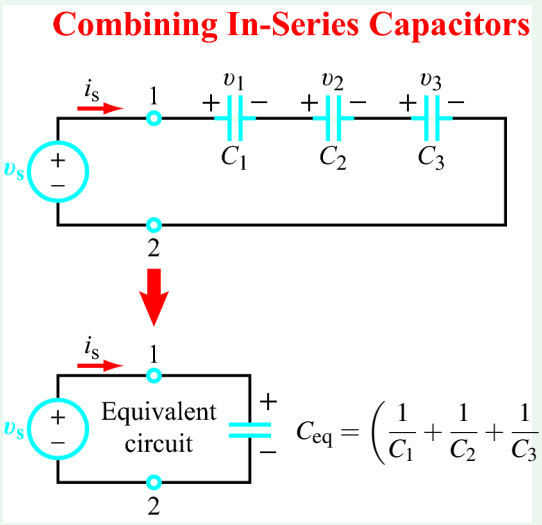


Figure 5.16 Capacitors in series.

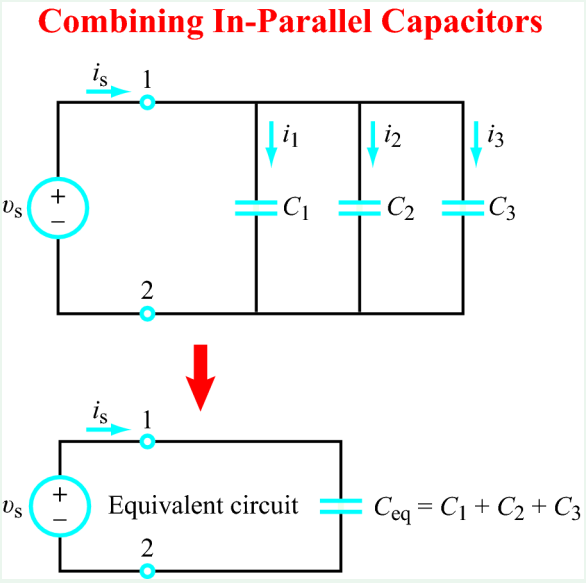


Figure 5.17 Capacitors in parallel.

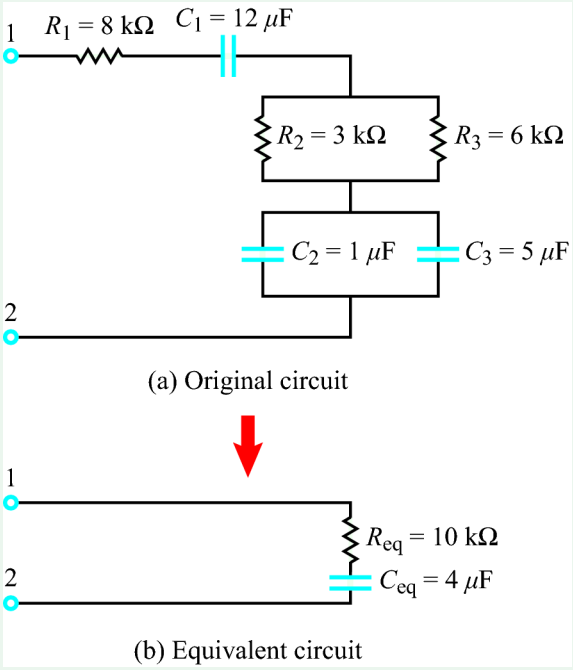
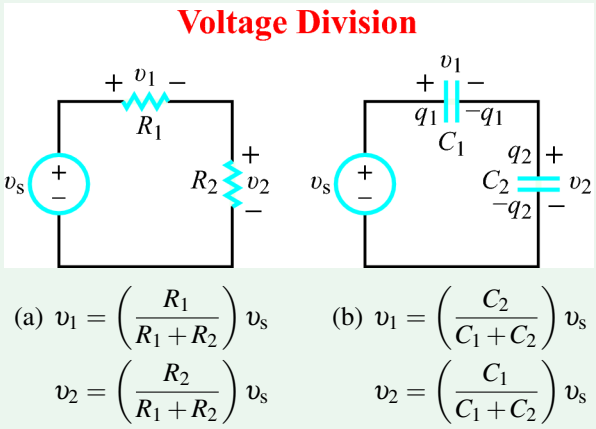


Figure 5.18 Circuit for Example 5-5.



(a) $v_1 = \left(\frac{R_1}{R_1 + R_2}\right) v_s$

$v_2 = \left(\frac{R_2}{R_1 + R_2}\right) v_s$

(b) $v_1 = \left(\frac{C_2}{C_1 + C_2}\right) v_s$

$v_2 = \left(\frac{C_1}{C_1 + C_2}\right) v_s$

Figure 5.19 Voltage-division rules for (a) in-series resistors and (b) in-series capacitors.

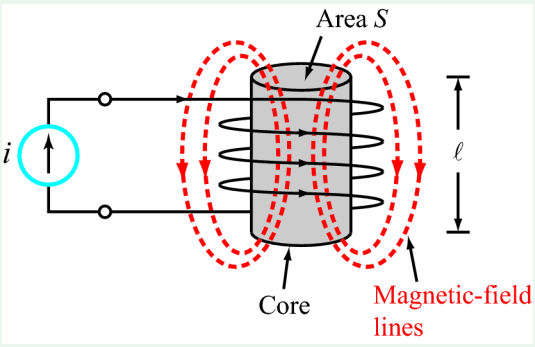
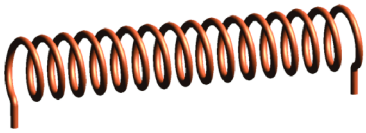


Figure 5.20 The inductance of a solenoid of length ℓ and cross-sectional area S is $L = \mu N^2 S/\ell$, where N is the number of turns and μ is the magnetic permeability of the core material.

High current inductor

Planar inductor



Solenoid

Figure 5.21 Various types of inductors.

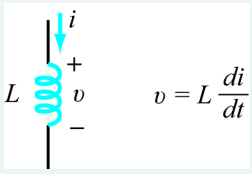


Figure 5.22 Passive sign convention for an inductor.

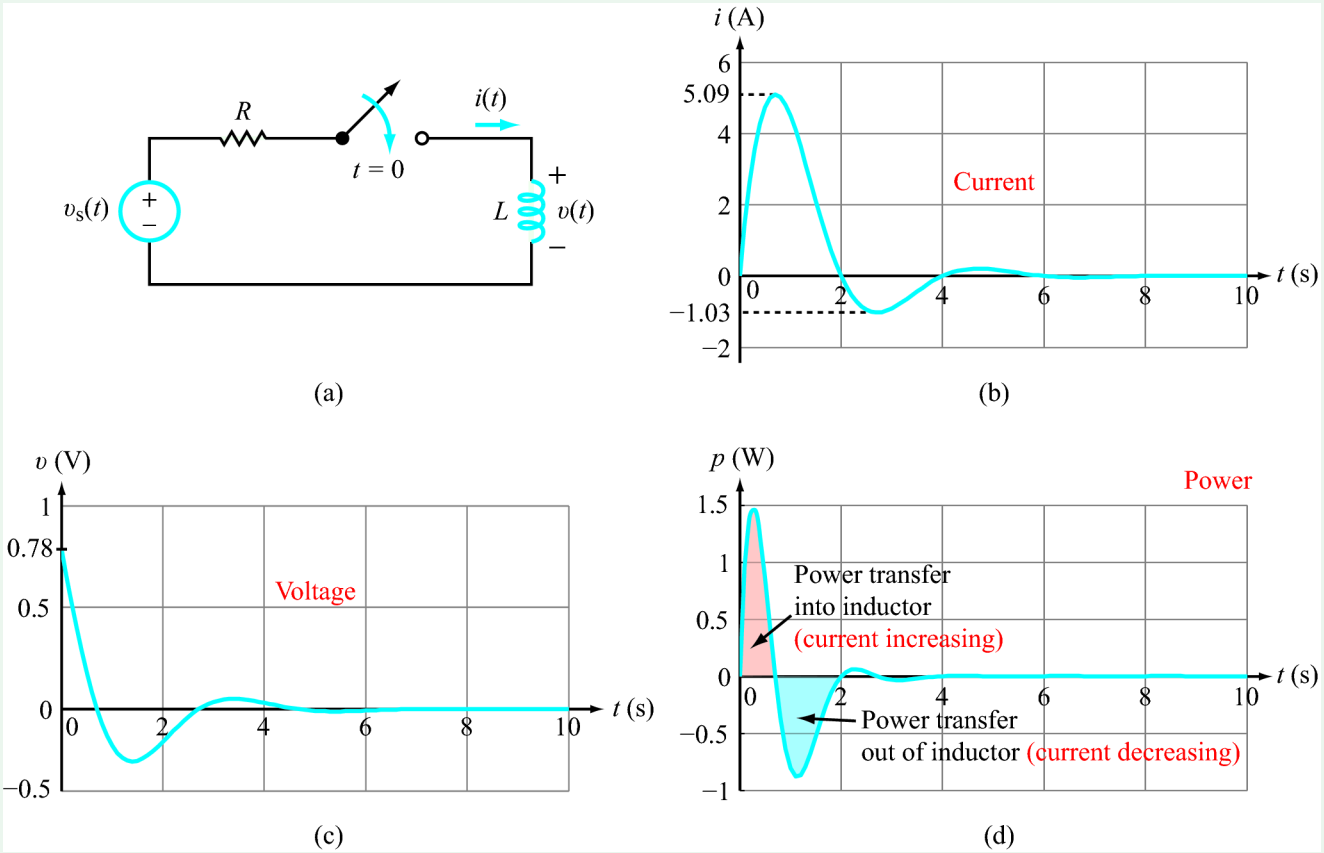


Figure 5.23 Circuit for Example 5-7.

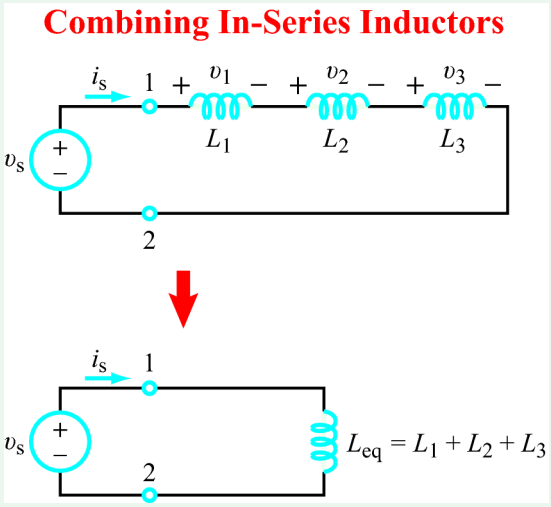
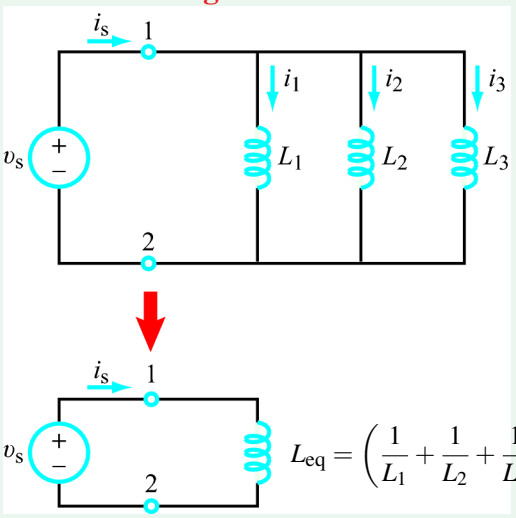


Figure 5.24 Inductors in series.

Combining In-Parallel Inductors



$$L_{eq} = \left(\frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3}\right)^{-1}$$

Figure 5.25 Inductors in parallel.

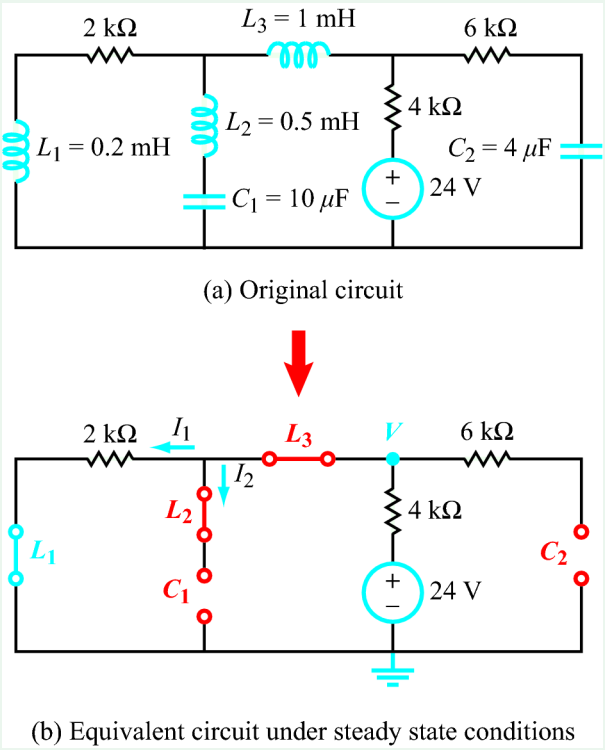


Figure 5.26 Under steady-state dc conditions, capacitors act like open circuits, and inductors act like short circuits.

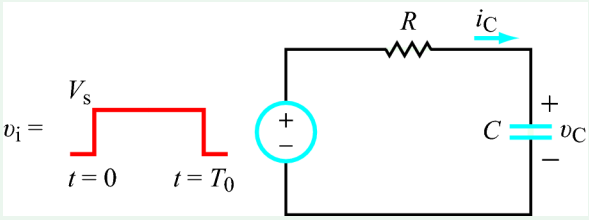


Figure 5.27 Generic first-order RC circuit.

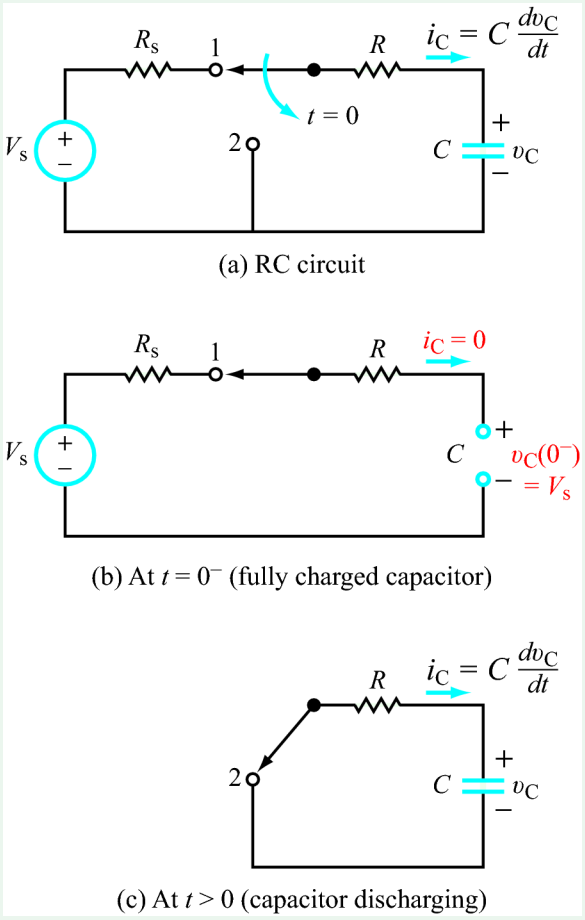


Figure 5.28 RC circuit with an initially charged capacitor that starts to discharge its energy after $t = 0$.

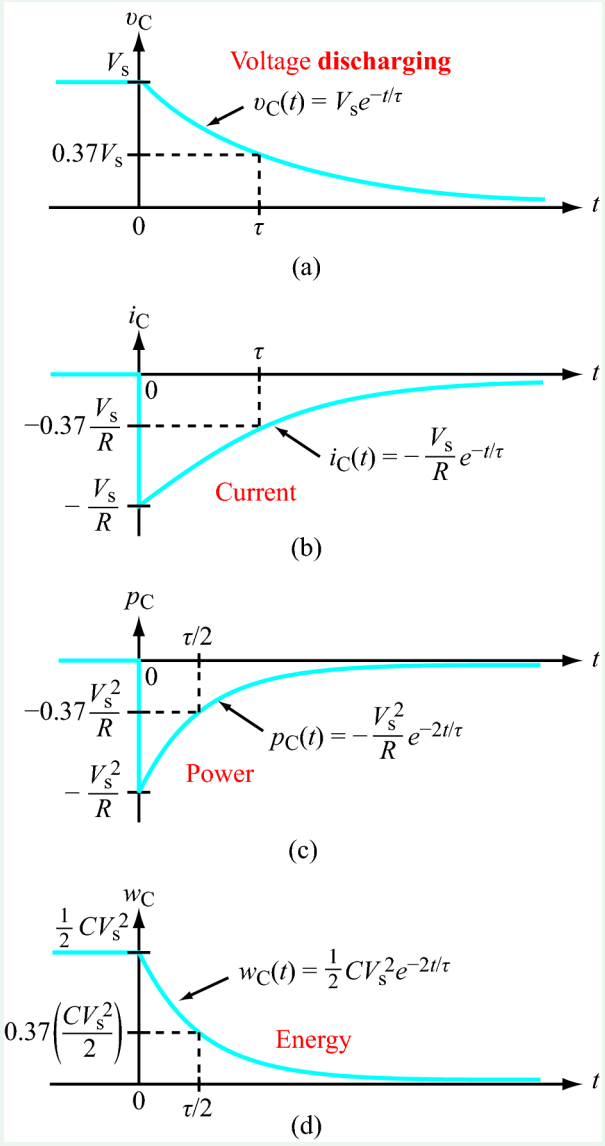


Figure 5.29 Response of the RC circuit in **Fig. 5.28(a)** to moving the SPDT switch to terminal 2.

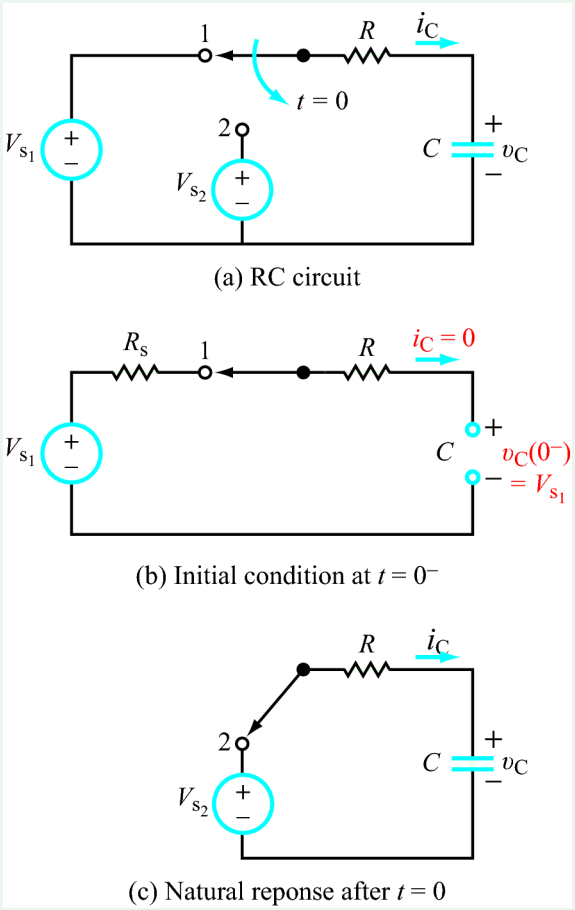


Figure 5.30 RC circuit switched from source V_{s_1} to source V_{s_2} at $t = 0$.

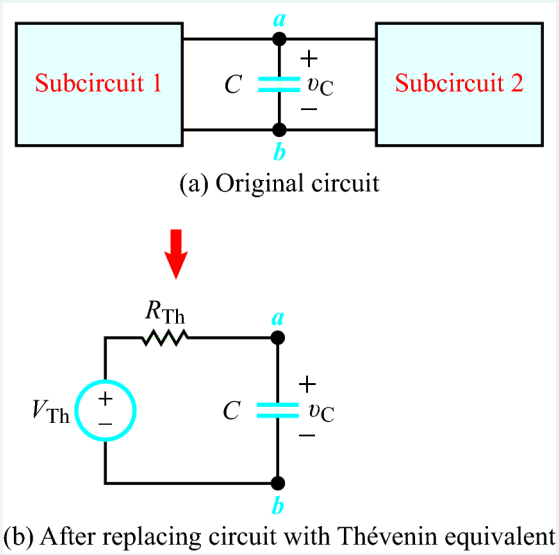


Figure 5.31 Replacing a resistive circuit with its Thévenin equivalent as seen by capacitor *C*.

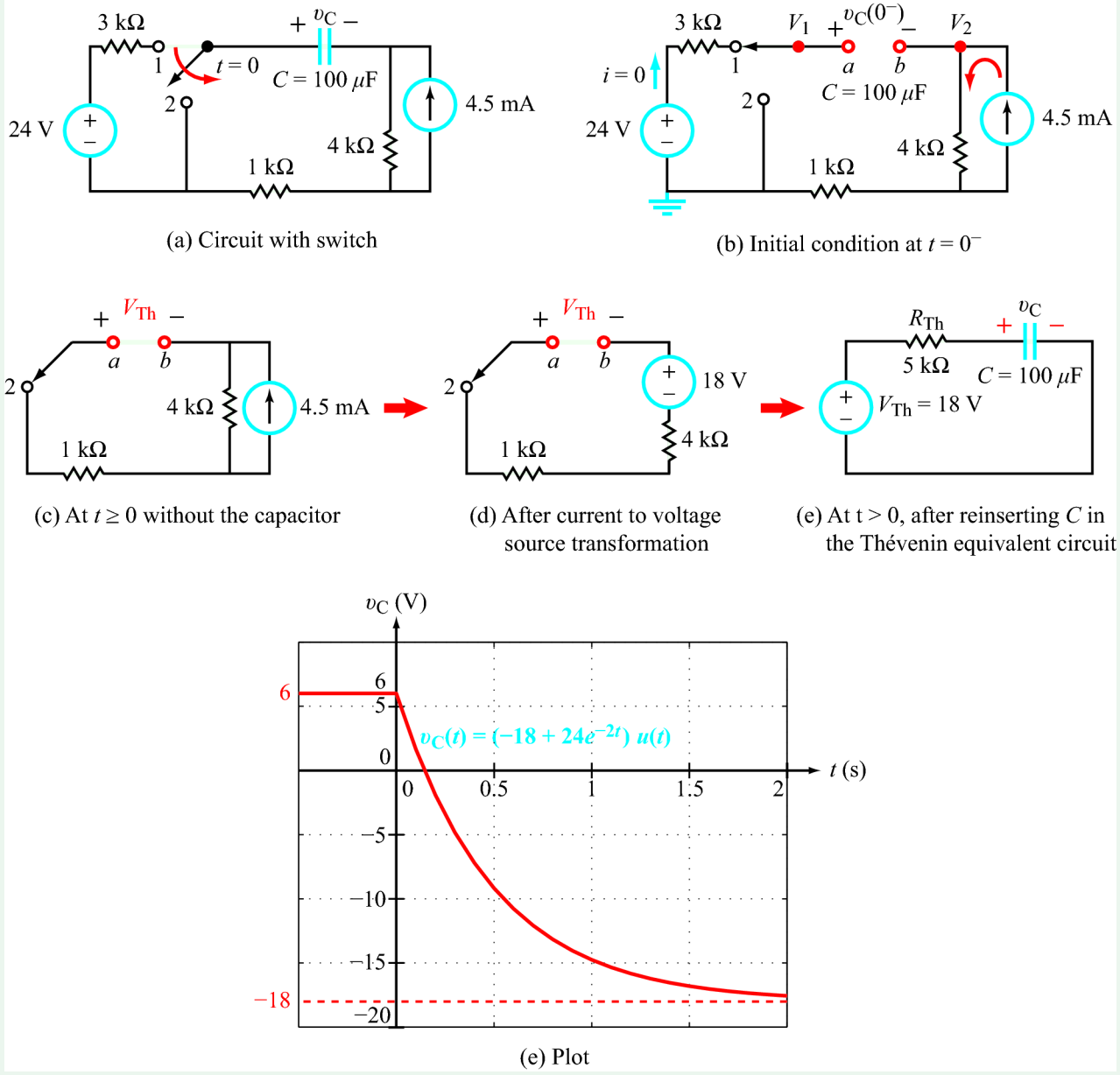


Figure 5.32 Circuit for Example 5-9.

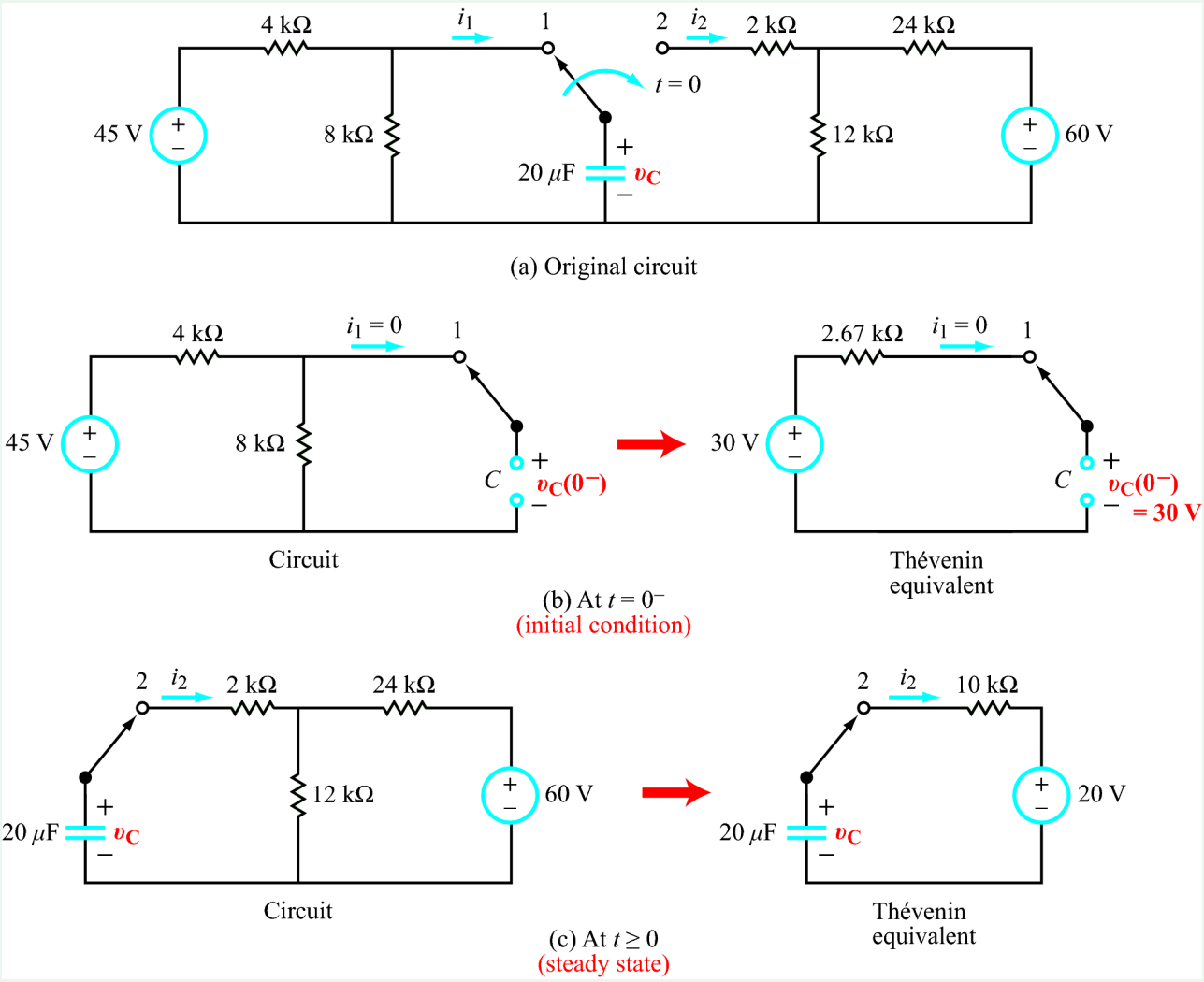


Figure 5.33 Circuit for Example 5-10 [part (a)].

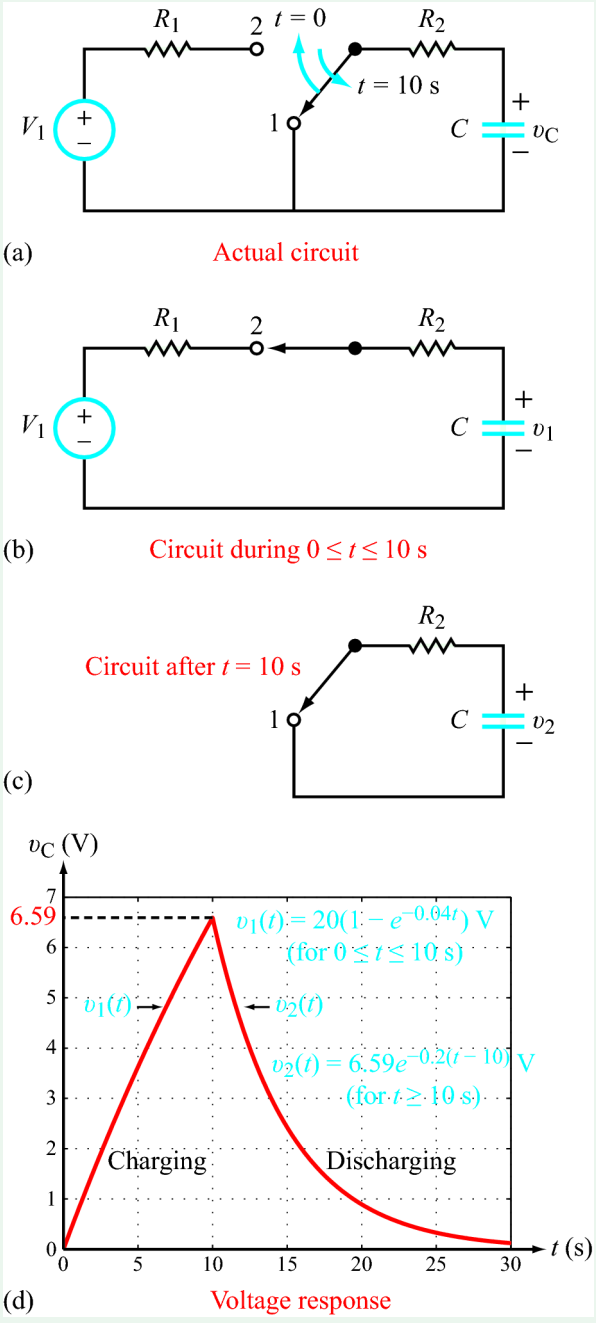


Figure 5.34 After having been in position 1 for a long time, the switch is moved to position 2 at $t = 0$ and then returned to position 1 at $t = 10$ s (Example 5-11).

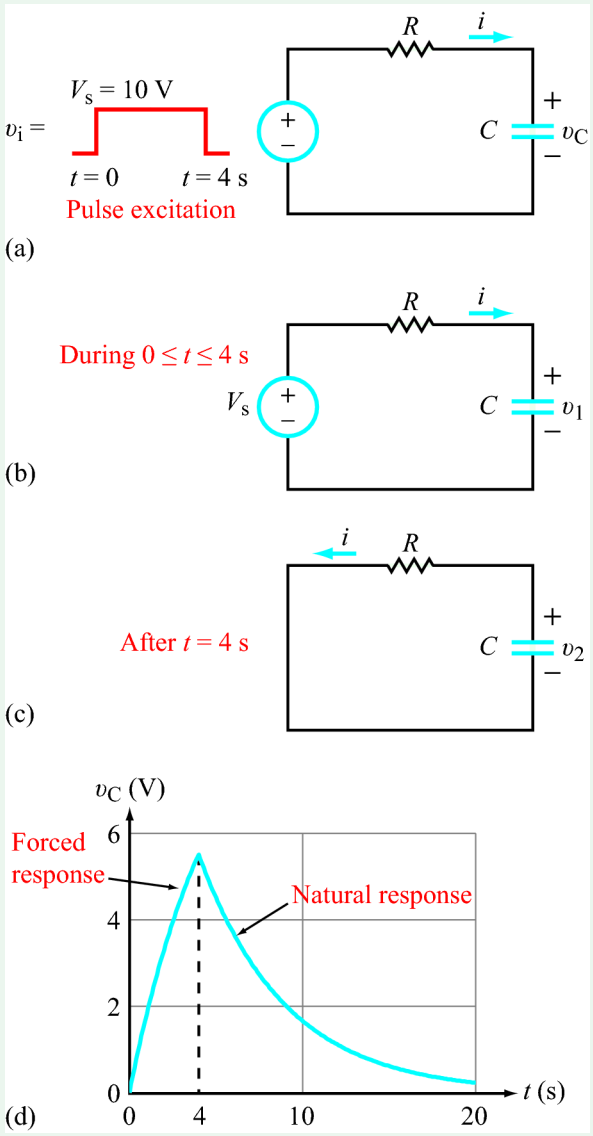


Figure 5.35 RC-circuit response to a 4 s long rectangular pulse.

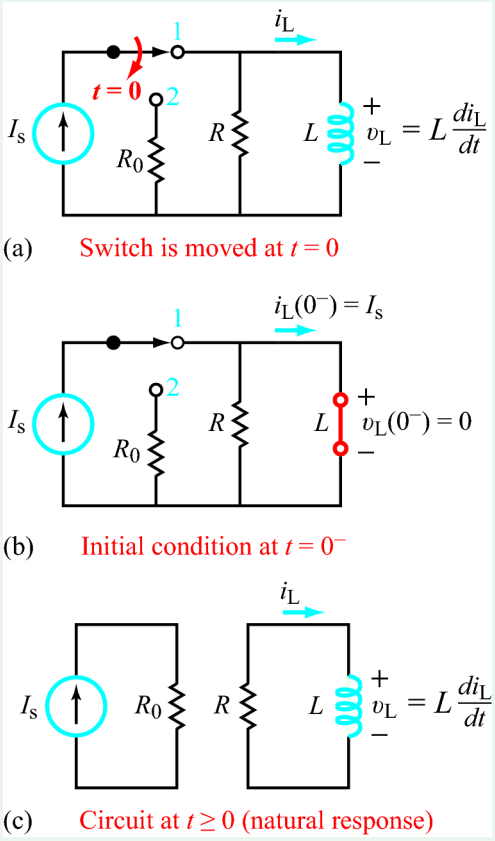


Figure 5.36 RL circuit disconnected from a current source at $t = 0$.

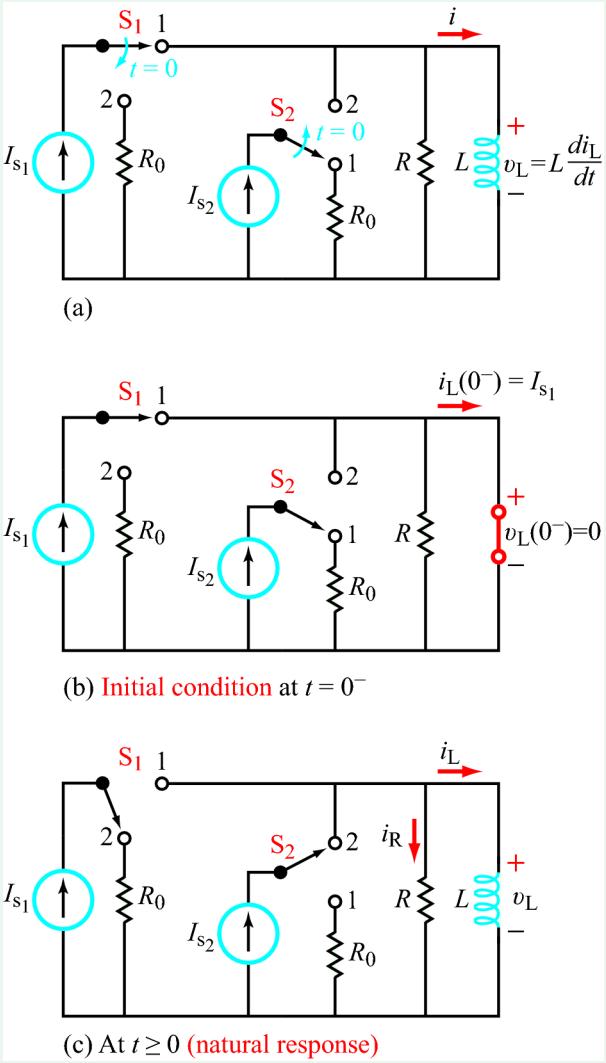


Figure 5.37 RL circuit switched between two current sources at $t = 0$.

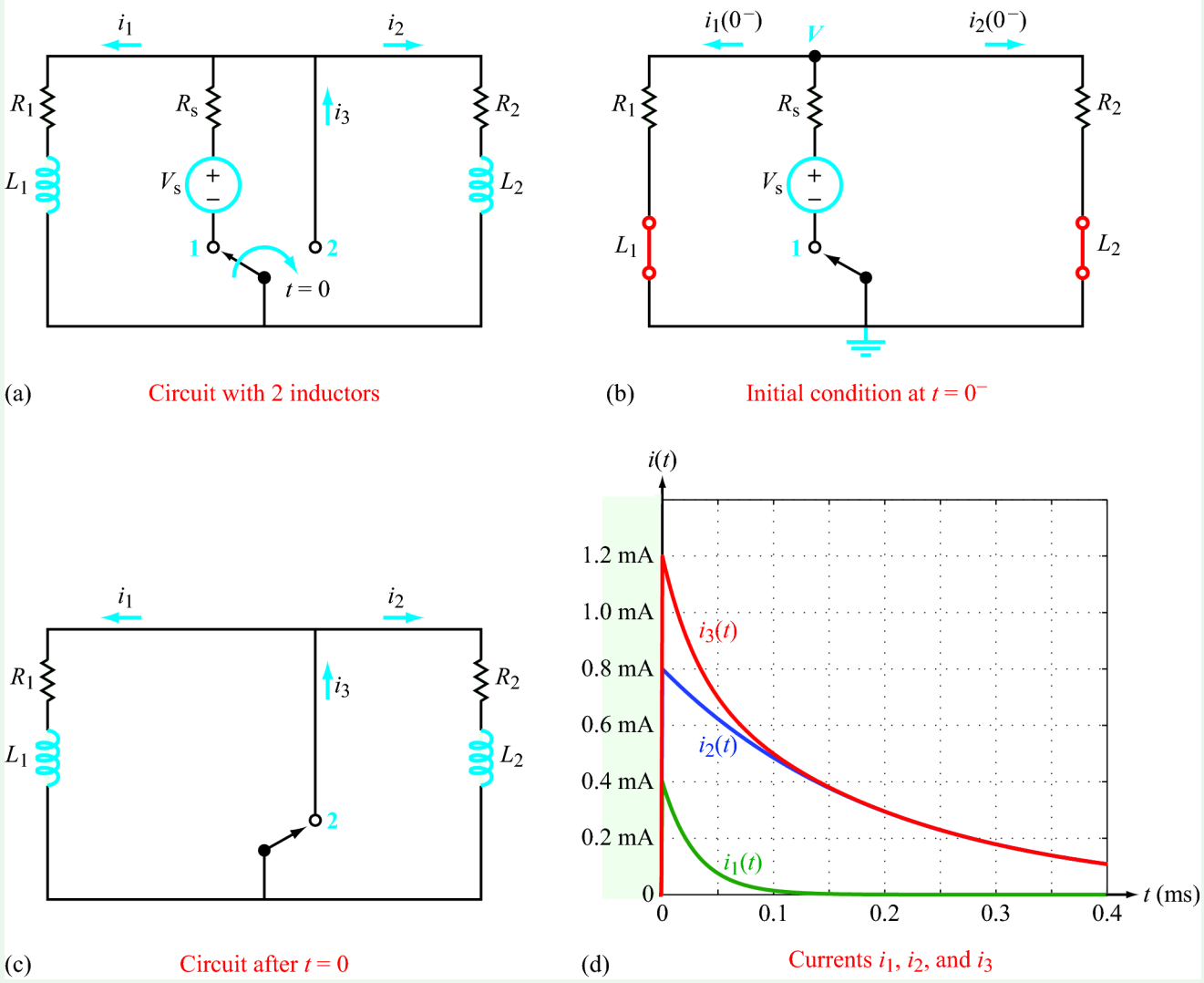


Figure 5.38 Circuit for Example 5-13.

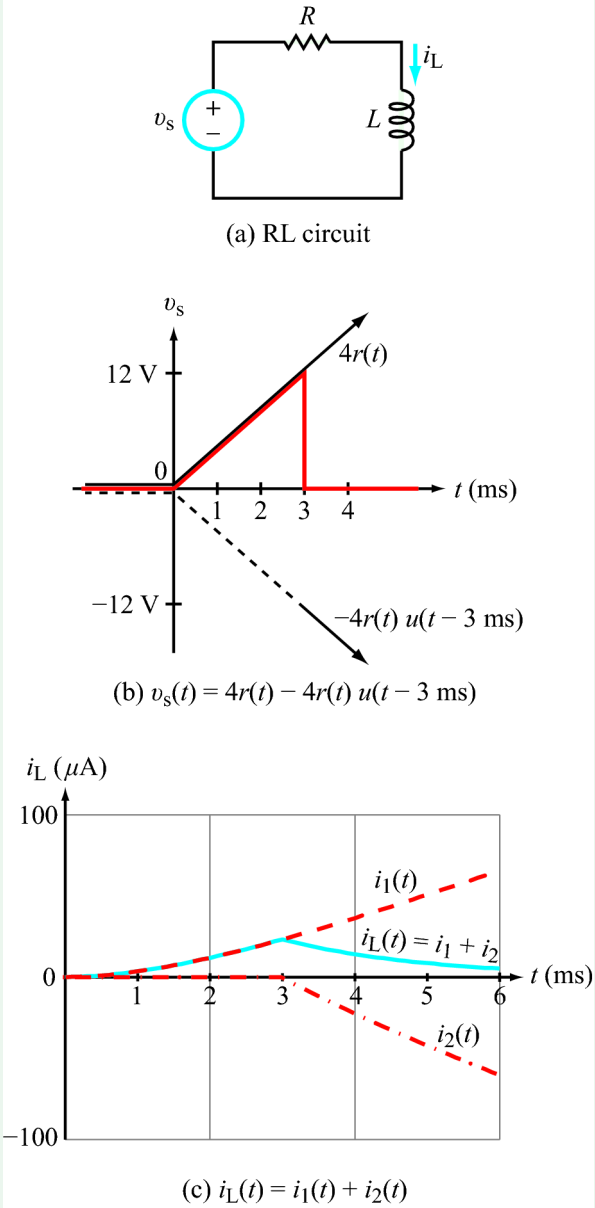


Figure 5.39 Circuit and associated plot for Example 5-14.

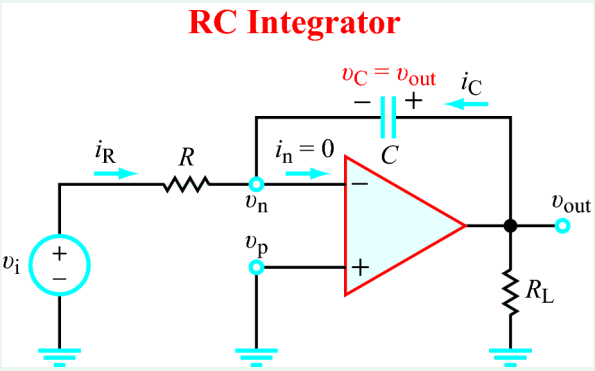


Figure 5.40 Integrator circuit.

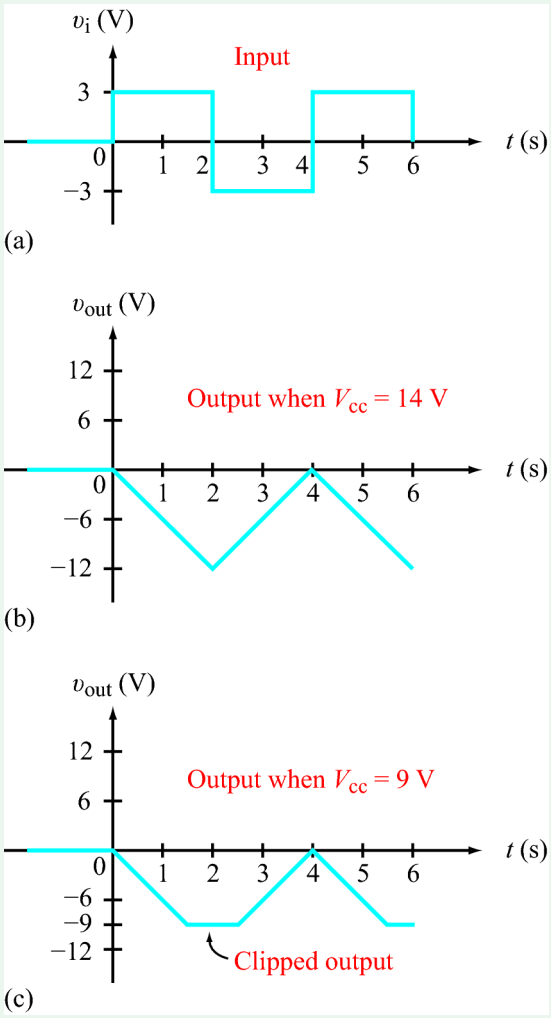


Figure 5.41 Example 5-15 (a) input signal, (b) output signal with no op-amp saturation, and (c) output signal with op-amp saturation at −9 V.

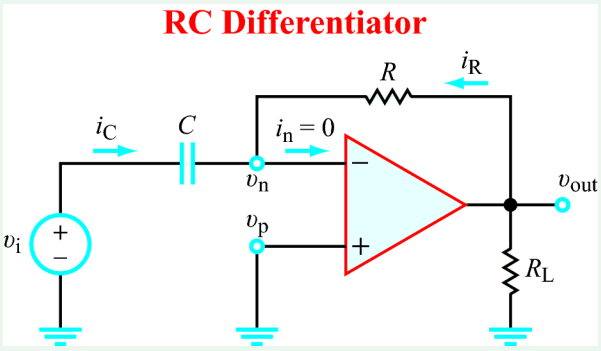


Figure 5.42 Differentiator circuit.

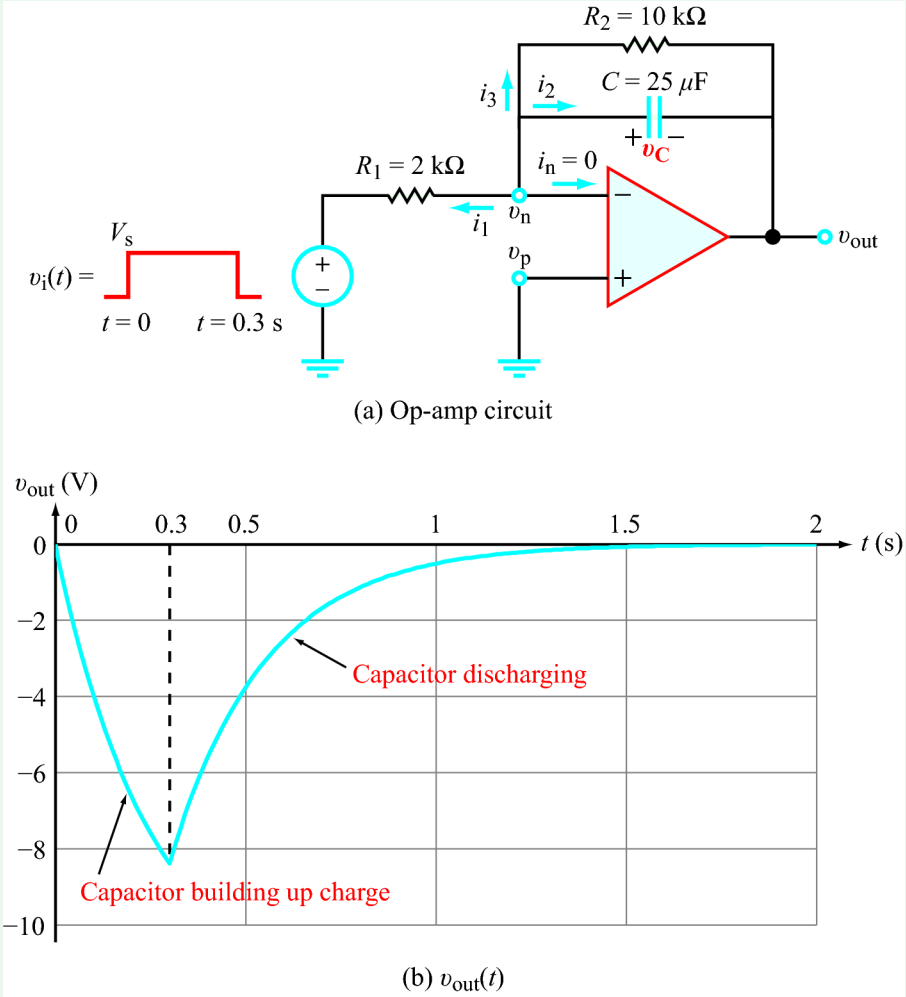


Figure 5.43 Op-amp circuit of Example 5-16.

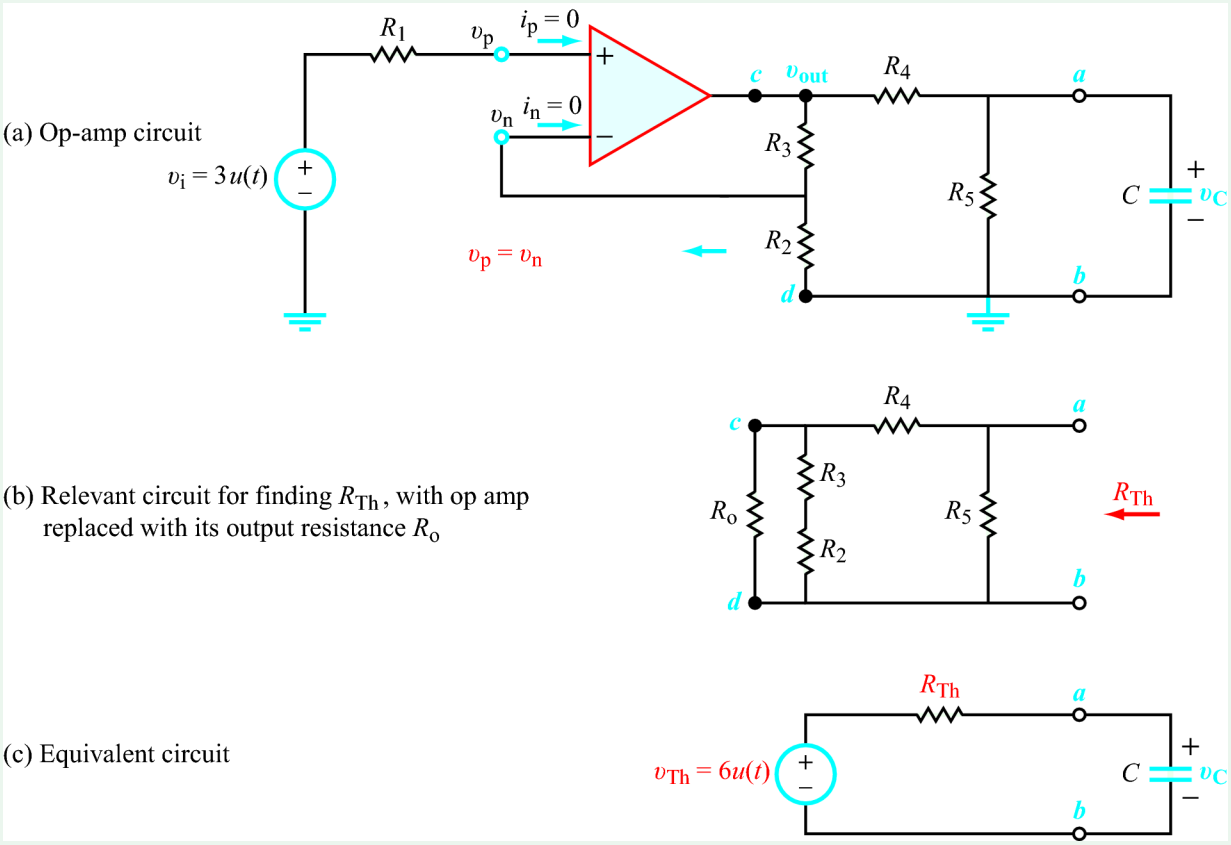


Figure 5.44 Circuit for Example 5-17.

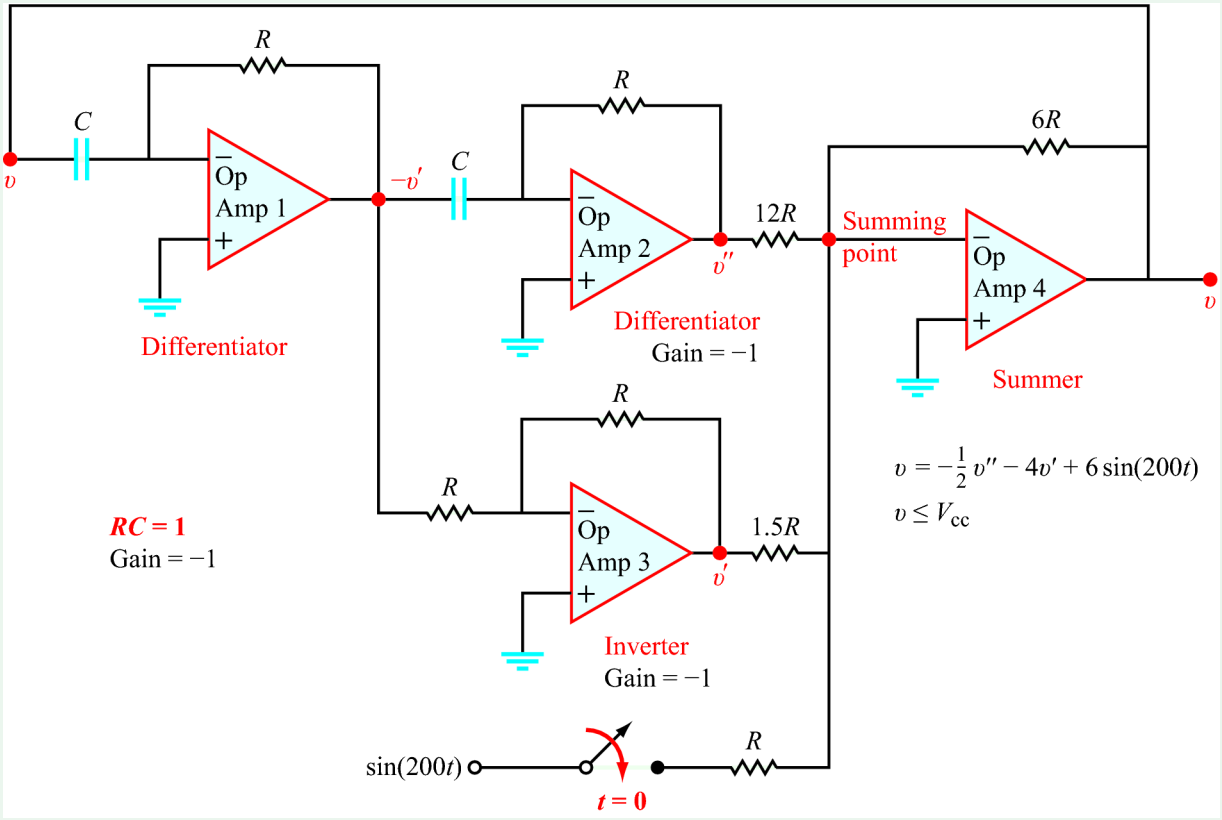


Figure 5.45 Op-amp circuit whose output $v(t)$ is a solution to $v'' + 8v' + 2v = 12\sin(200t)\,u(t)$.

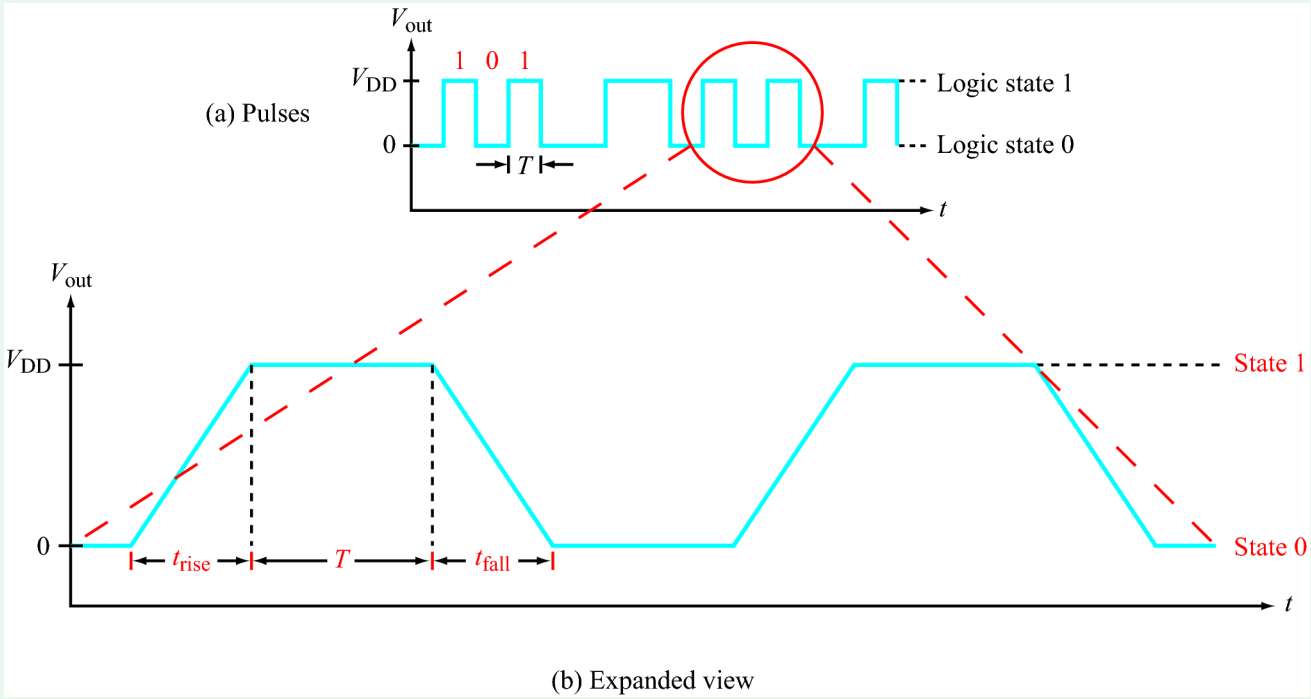
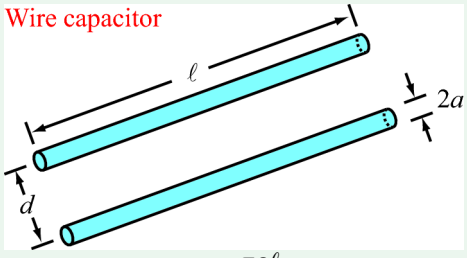


Figure 5.46 Pulse sequence.



$$C = \frac{\pi\varepsilon\ell}{\ln[(d/2a) + \sqrt{(d/2a)^2 - 1}]}$$
$$\approx \frac{\pi\varepsilon\ell}{\ln(d/a)} \qquad \text{if } d \gg a$$

Figure 5.47 Capacitance of a two-wire configuration where ε is the permittivity of the material separating the wires.

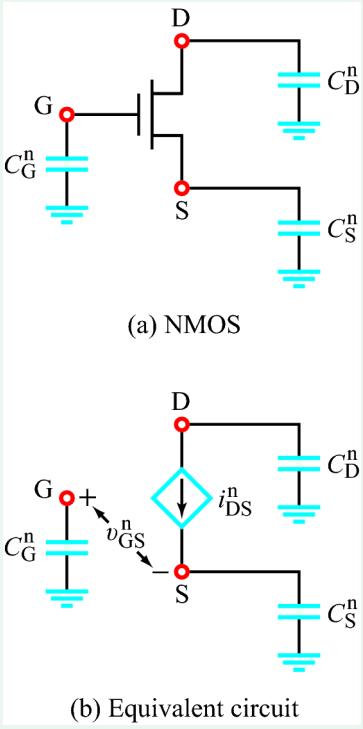
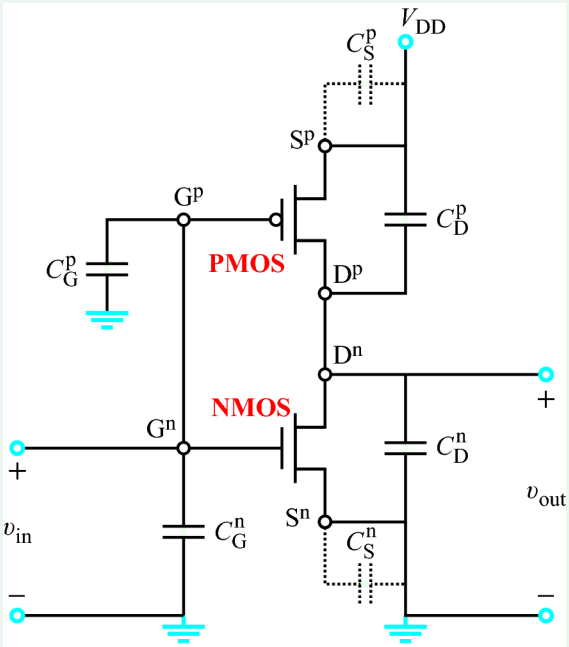
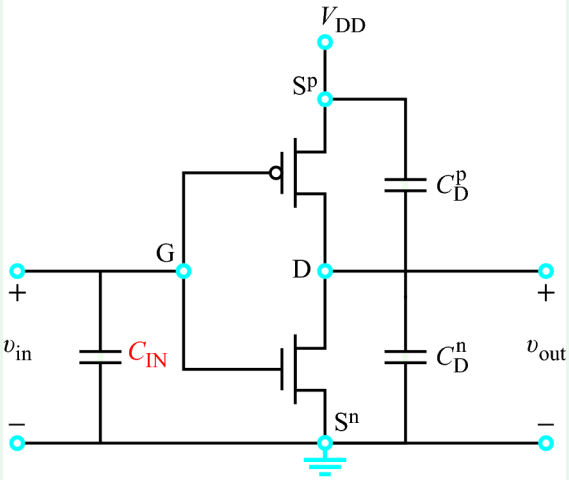


Figure 5.48 n-channel MOSFET (NMOS): (a) circuit symbol with added parasitic capacitances and (b) equivalent circuit. [In a PMOS, parasitic capacitances C_D^p and C_S^p should be shown connected to V_{DD} instead of to ground.]



(a) Original circuit



(b) Simplified circuit

Figure 5.49 Common drain inverter circuit with parasitic capacitances. Superscripts "n" and "p" refer to the NMOS and PMOS transistors, respectively.

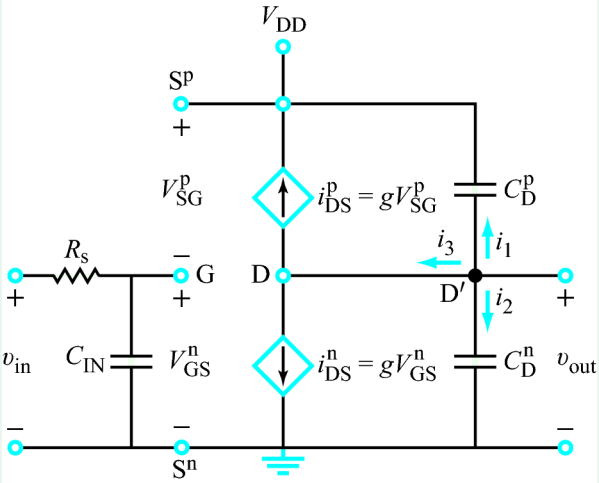


Figure 5.50 (a) Equivalent circuit for the CMOS inverter; (b) the response of $v_{out}(t)$ to v_{in} changing states from 0 to V_{DD} at $t = 0$.

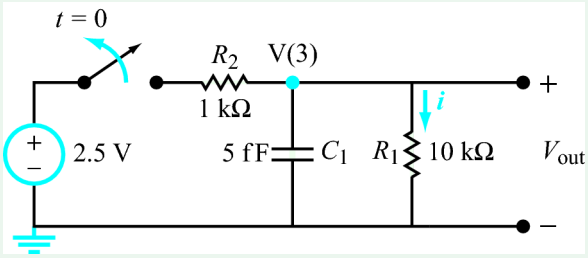


Figure 5.51 RC circuit with an SPST switch.

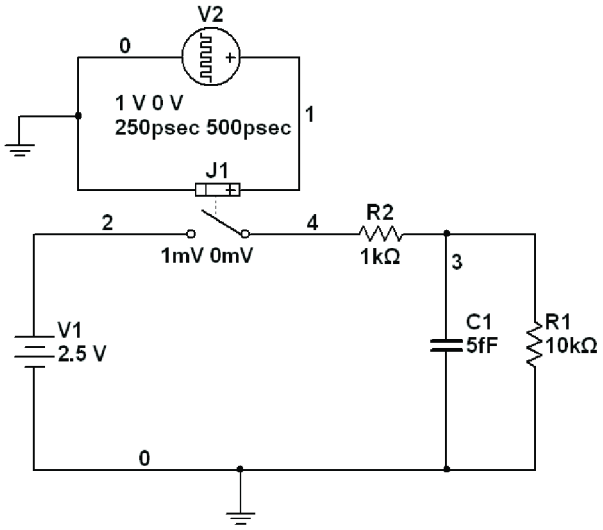


Figure 5.52 Multisim equivalent of the RC circuit in **Fig.** 5.51.

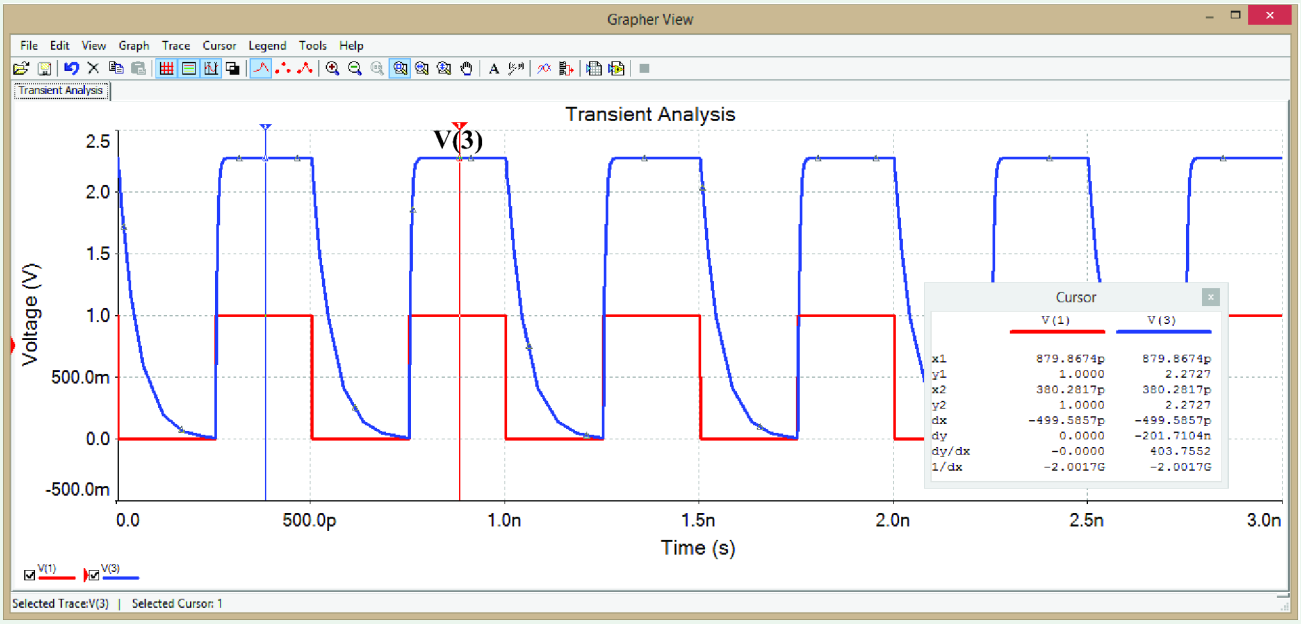
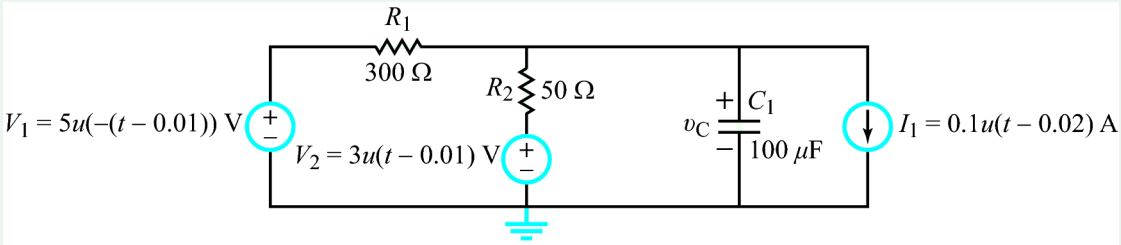
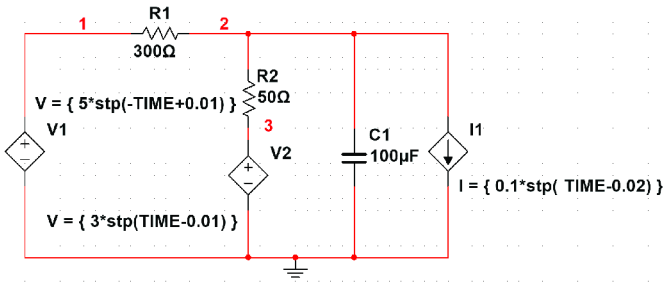


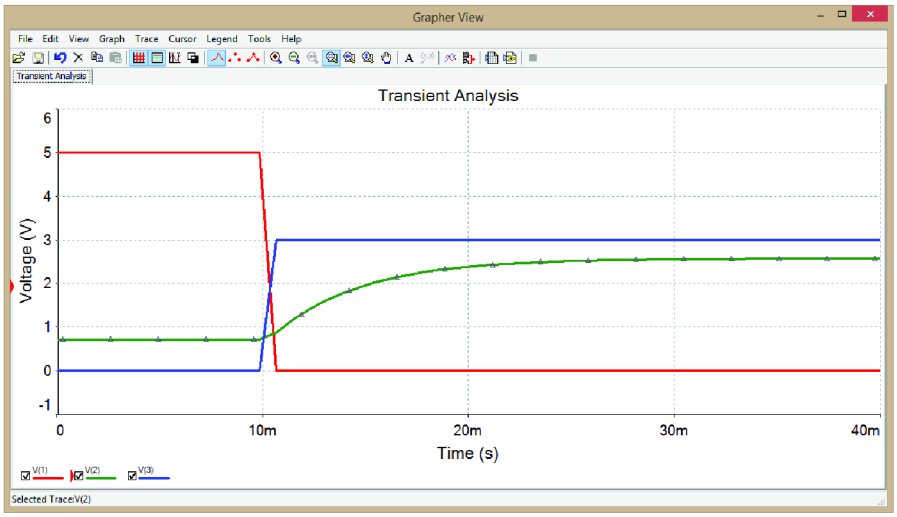
Figure 5.53 Transient response of the circuit in **Fig.** 5.52.



(a) Circuit with three time-dependent sources



(b) Multisim circuit



(c) Trace of $v_C(t)$

Figure 5.54 Multisim analysis of a circuit containing time-dependent sources.

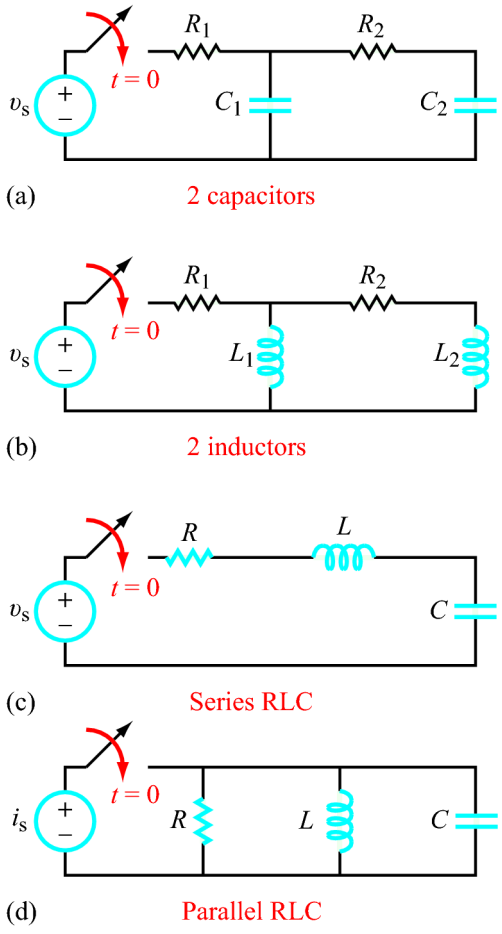
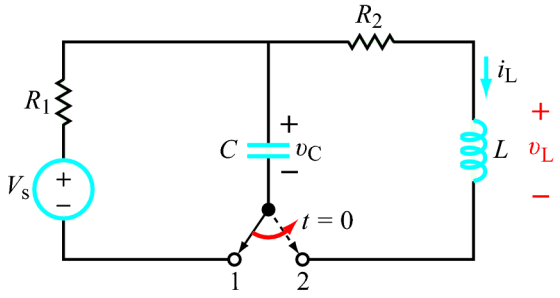
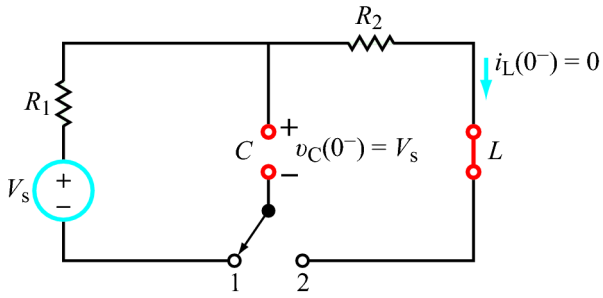


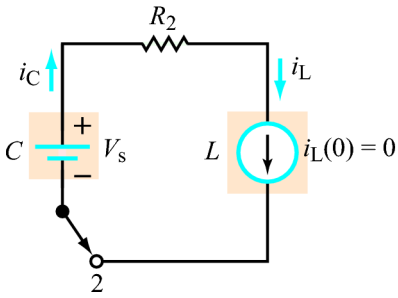
Figure 6.1 Examples of second-order circuits.



(a) Circuit



(b) At $t = 0^-$, C acts like an open circuit and L like a short circuit



(c) At $t = 0$, C acts like a voltage source and L like a current source with zero current

Figure 6.2 Circuit of Example 6-1.

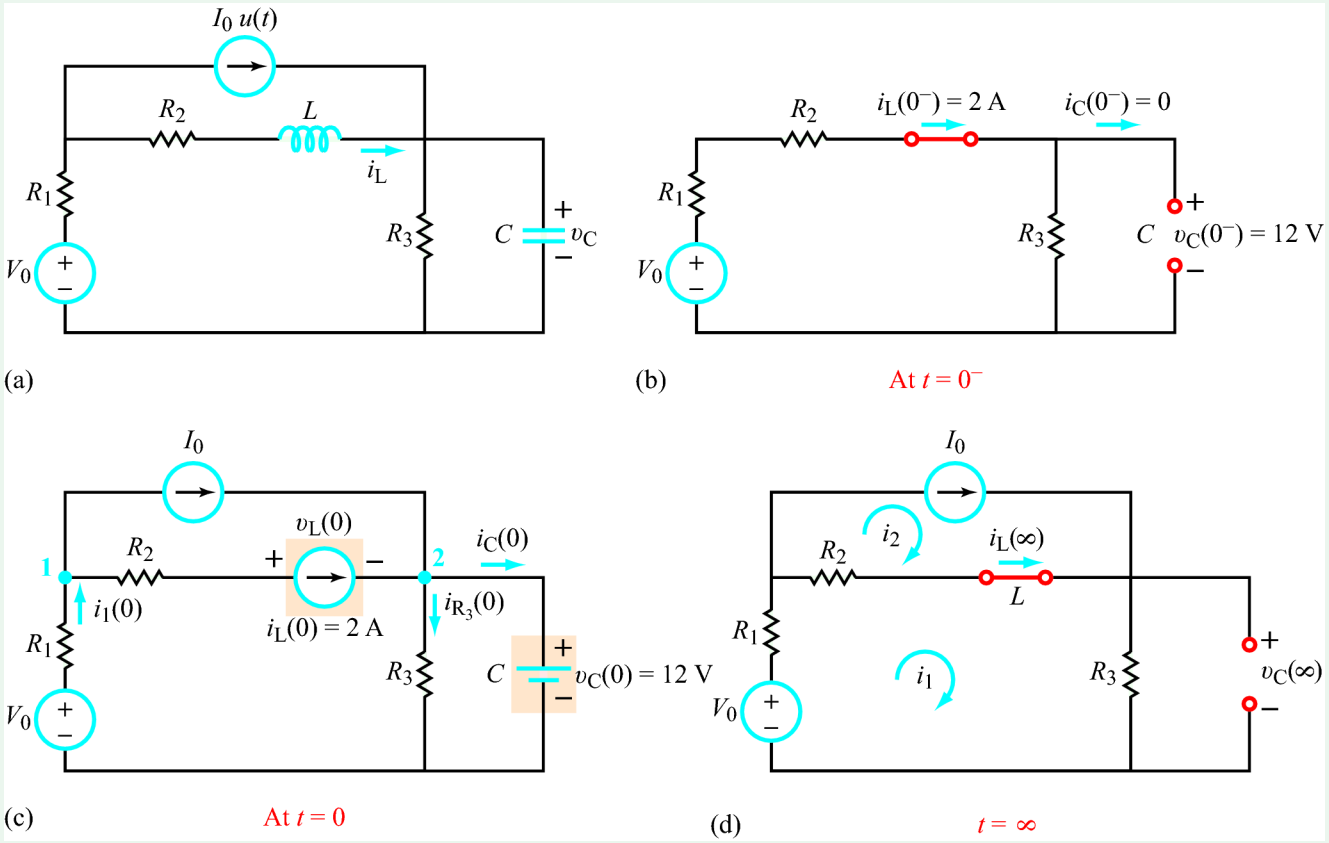
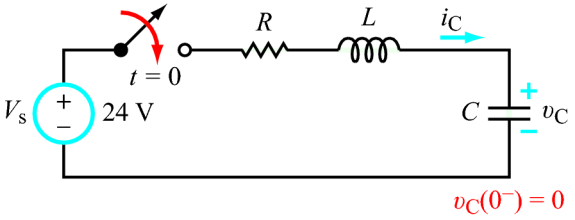
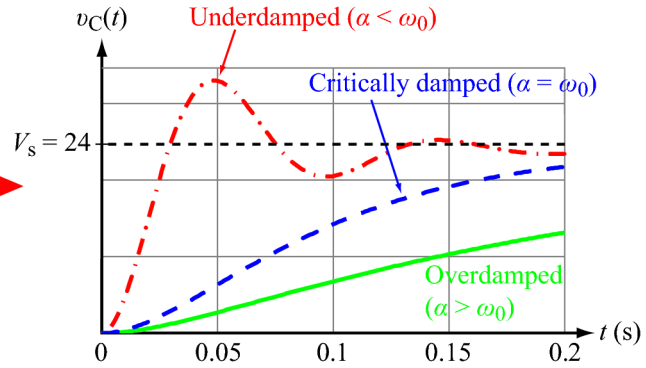


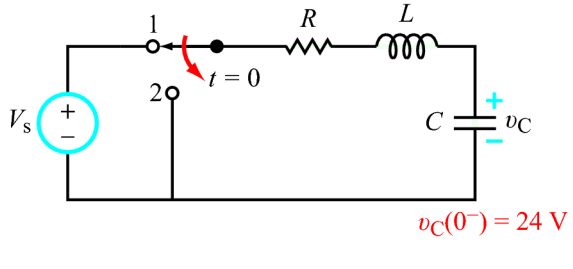
Figure 6.3 Circuit for Example 6-2.



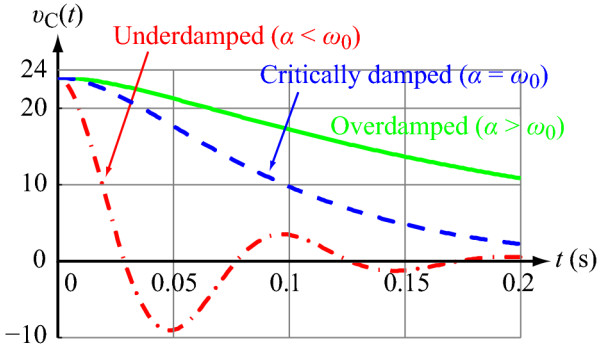
(a) Charging up C



(b) Responses



(c) Discharging C



(d) Responses

Figure 6.4 Illustrating the charge-up and discharge responses of a series RLC circuit with $V_s = 24$ V. In all cases $R = 12\ \Omega$ and $L = 0.3$ H, which specifies $\alpha = R/2L = 20$ Np/s. When $C = 0.01$ F, the response is overdamped, when $C = 8.33$ mF, the response is critically damped, and when $C = 0.72$ mF, the response is underdamped.

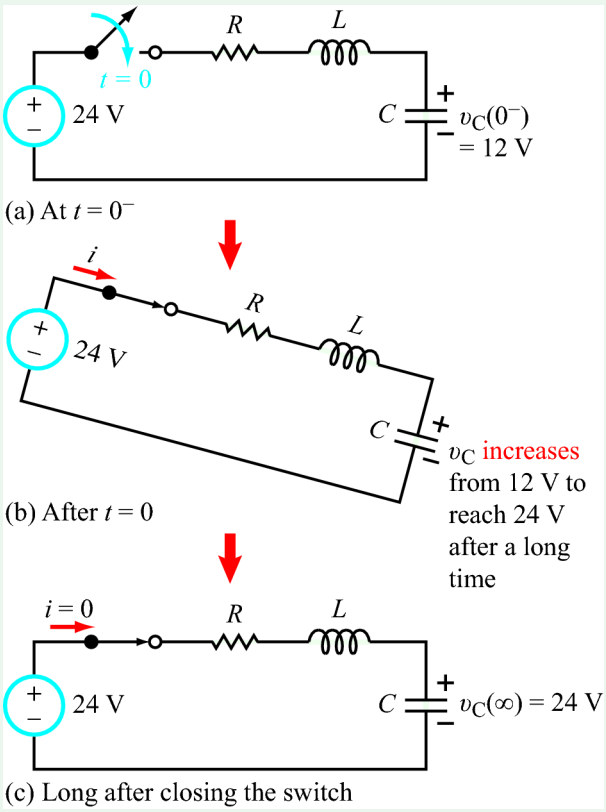


Figure 6.5 Connecting a series RLC circuit with a charged-up capacitor to a source with higher voltage.

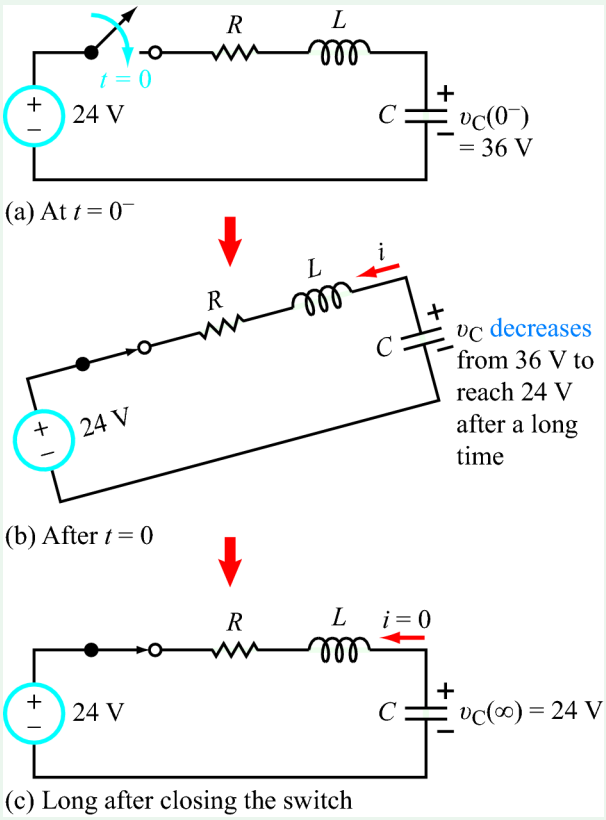


Figure 6.6 Connecting a series RLC circuit with a charged-up capacitor to a source with lower voltage.

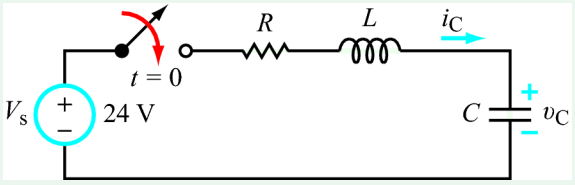


Figure 6.7 Series RLC circuit connected to a source V_s at $t = 0$. In general, the capacitor may have had an initial charge on it at $t = 0^-$, with a corresponding initial voltage $v_C(0^-)$.

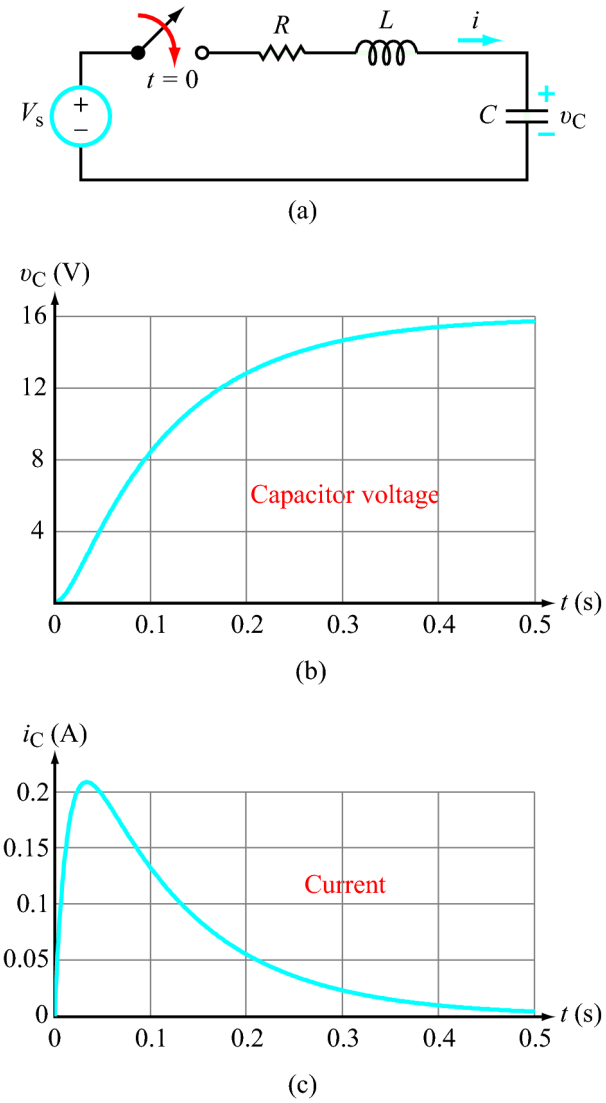


Figure 6.8 Example 6-3: (a) circuit, (b) $v_C(t)$, and (c) $i_C(t)$.

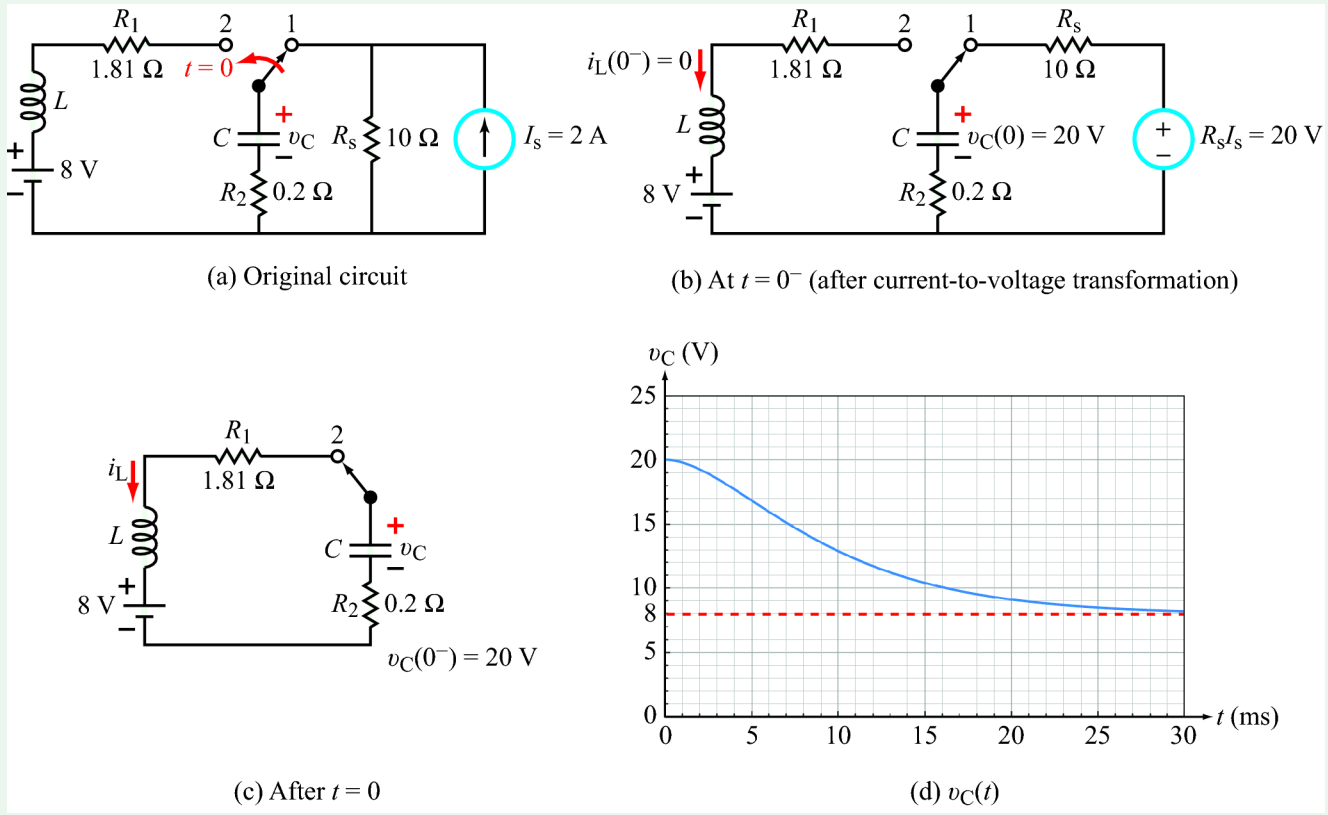


Figure 6.9 Circuit for Example 6-4.

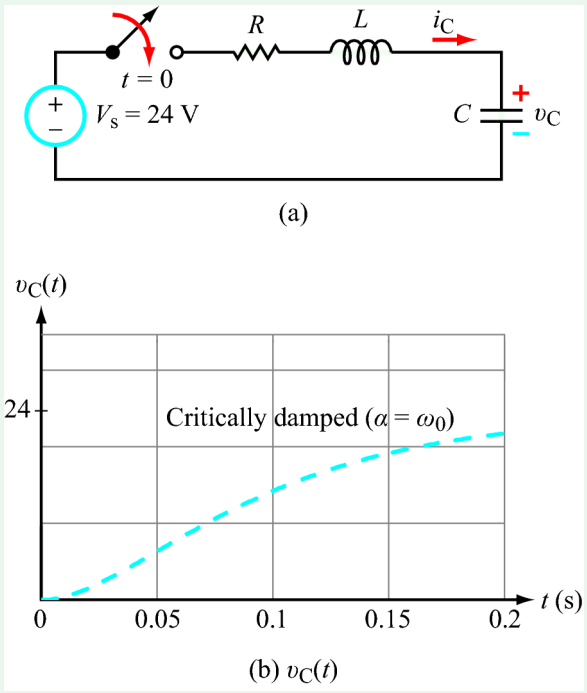
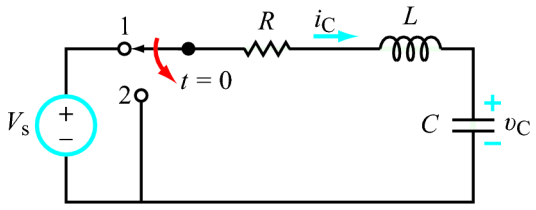
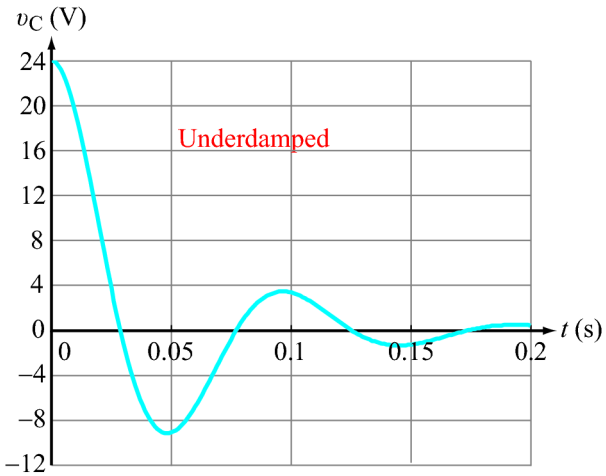


Figure 6.10 Circuit response for Example 6-5.



(a)



(b)

Figure 6.11 Example 6-6 (a) circuit and (b) $v_C(t)$.

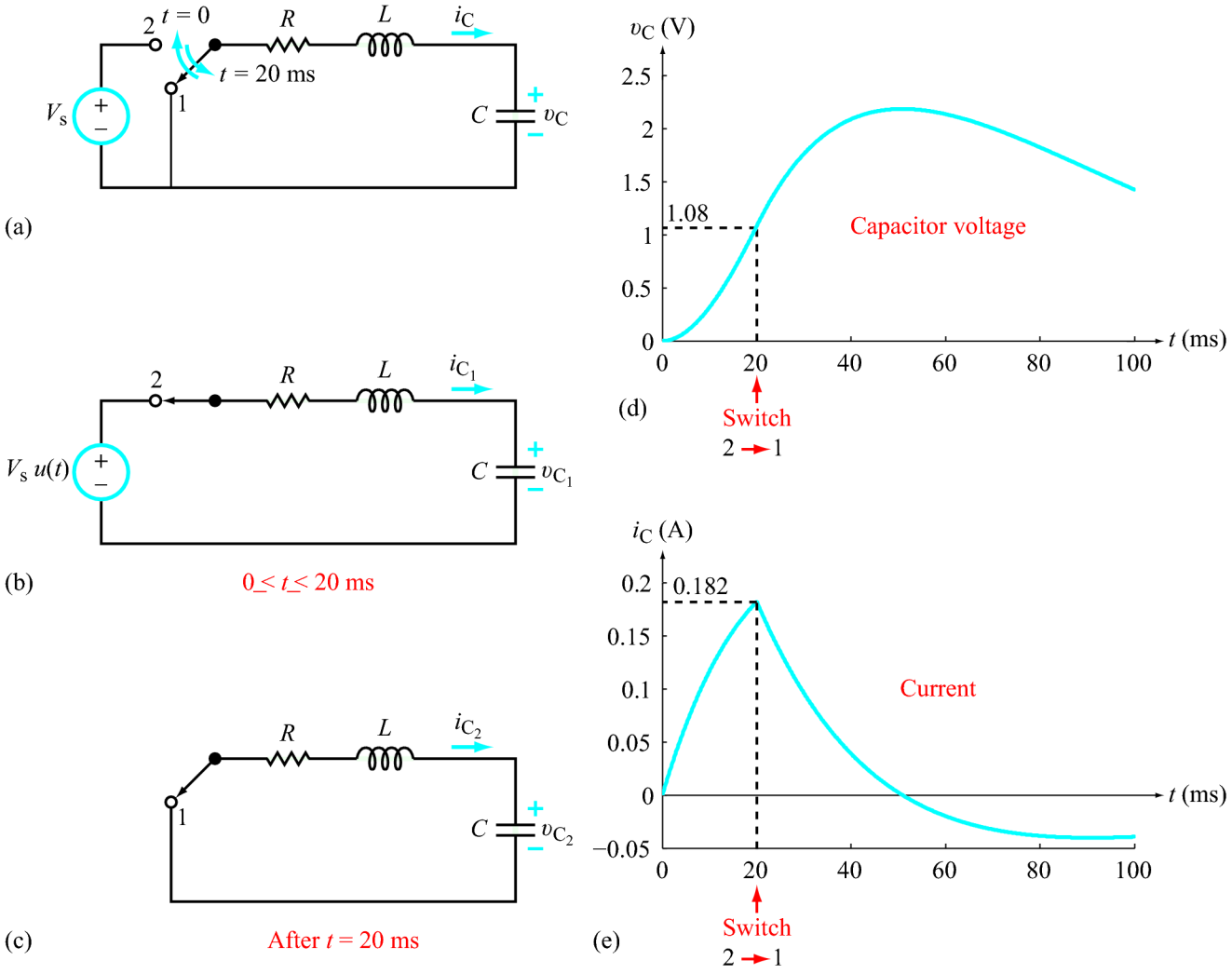


Figure 6.12 Example 6-7 with $V_s = 12$ V, $R = 40\ \Omega$, $L = 0.8$ H, and $C = 2$ mF.

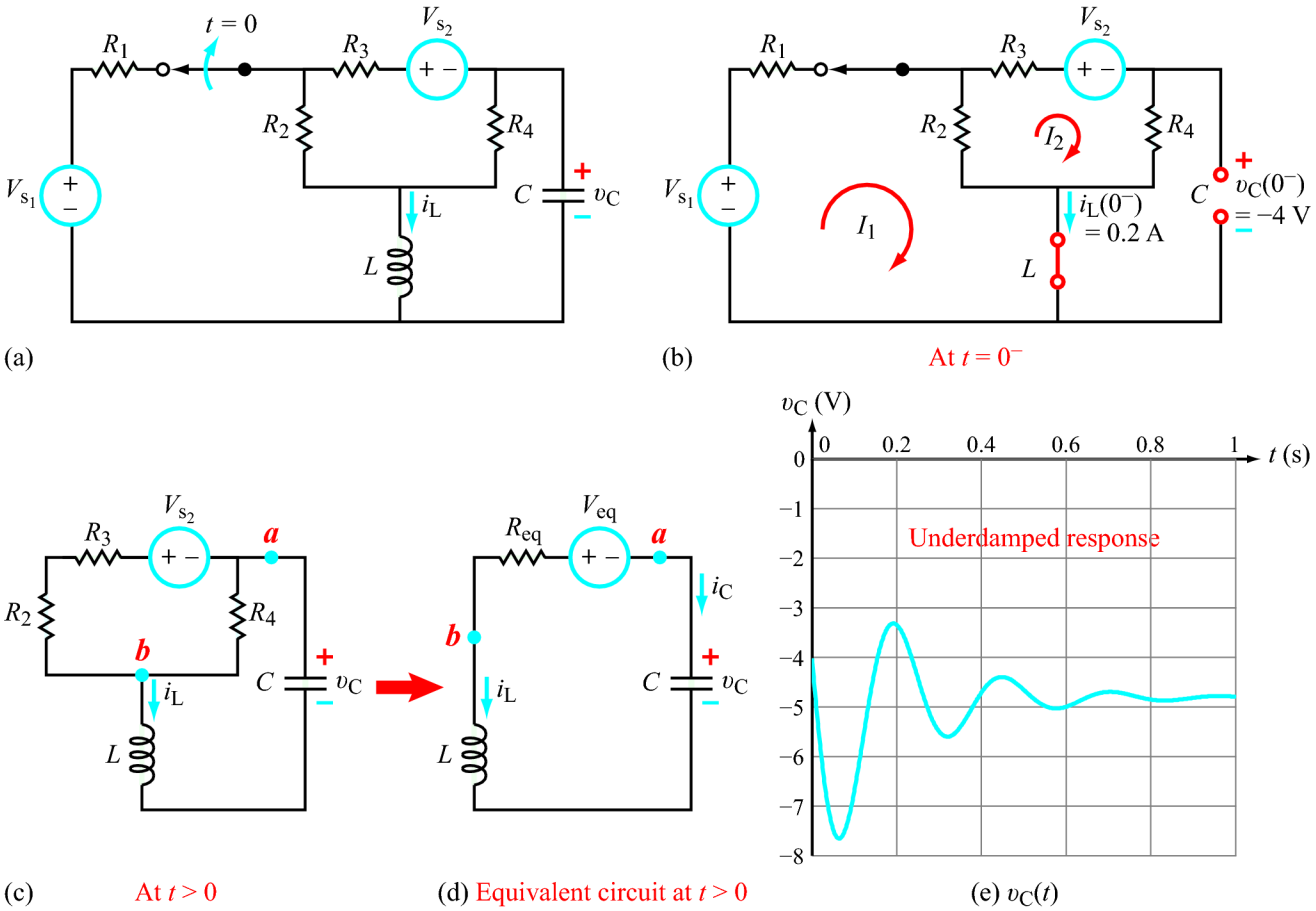
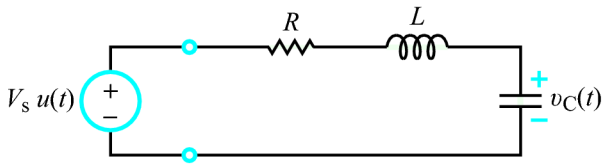
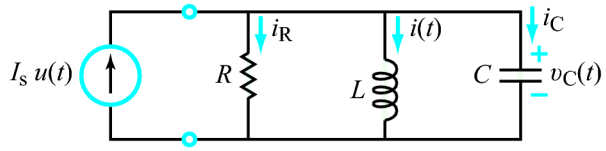


Figure 6.13 Circuit for Example 6-8.



(a) Series RLC



(b) Parallel RLC

Figure 6.14 The differential equation for $v_C(t)$ of the series RLC circuit shown in (a) is identical in form to that of the current $i_L(t)$ in the parallel RLC circuit in (b).

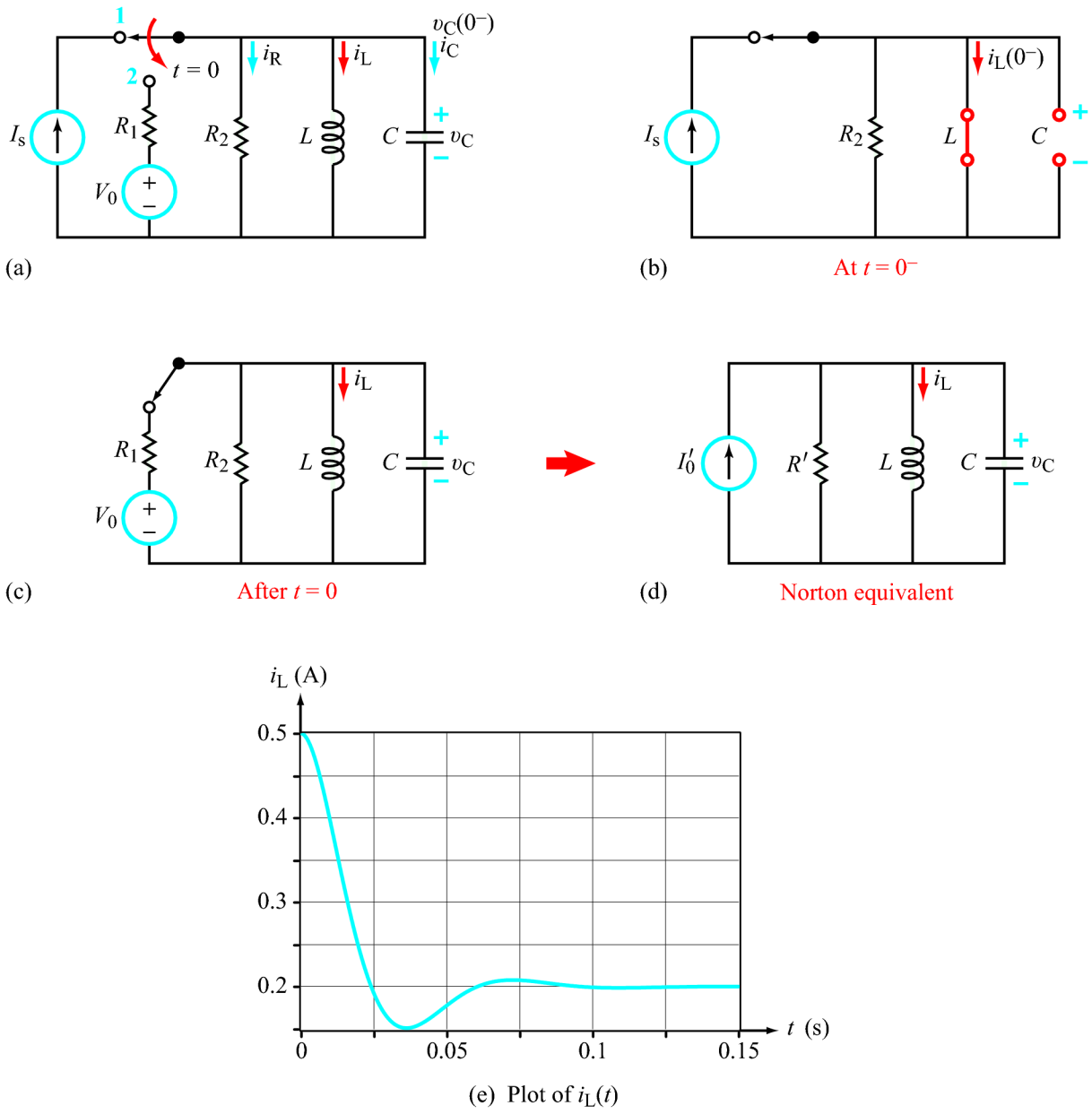
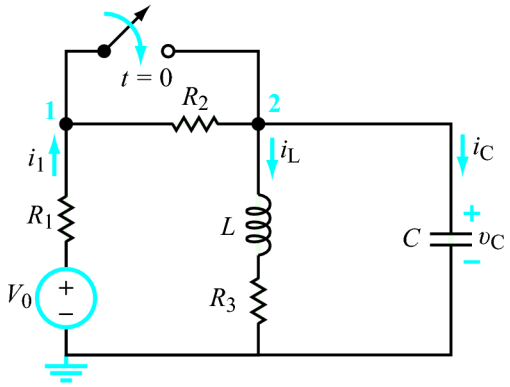
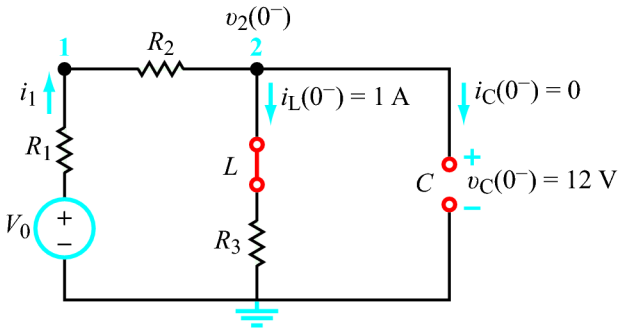


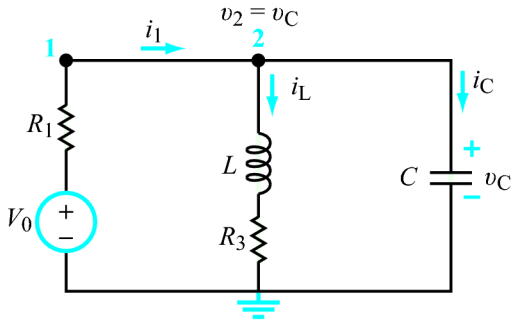
Figure 6.15 Circuit for Example 6-9.



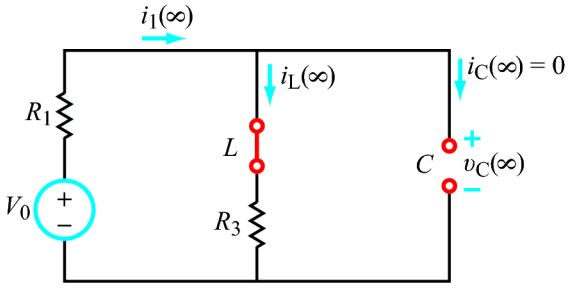
(a) Circuit with switch



(b) At $t = 0^-$: $i_L(0^-) = V_0/(R_1 + R_2 + R_3) = 1$ A, and $v_C(0^-) = i_L(0^-)\,R_3 = 12$ V.

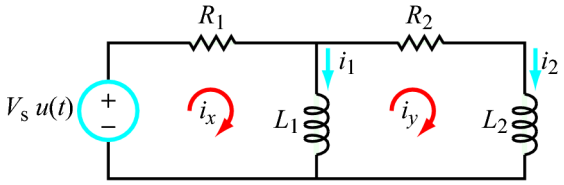


(c) At $t \geq 0$

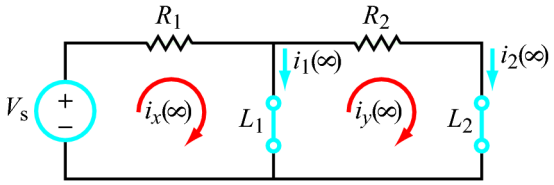


(d) At $t = \infty$: $i_L(\infty) = V_0/(R_1 + R_3) = 1.5$ A.

Figure 6.16 Circuit for Example 6-10.



(a) Circuit



(b) At $t = \infty$

Figure 6.17 Circuit for Example 6-11.

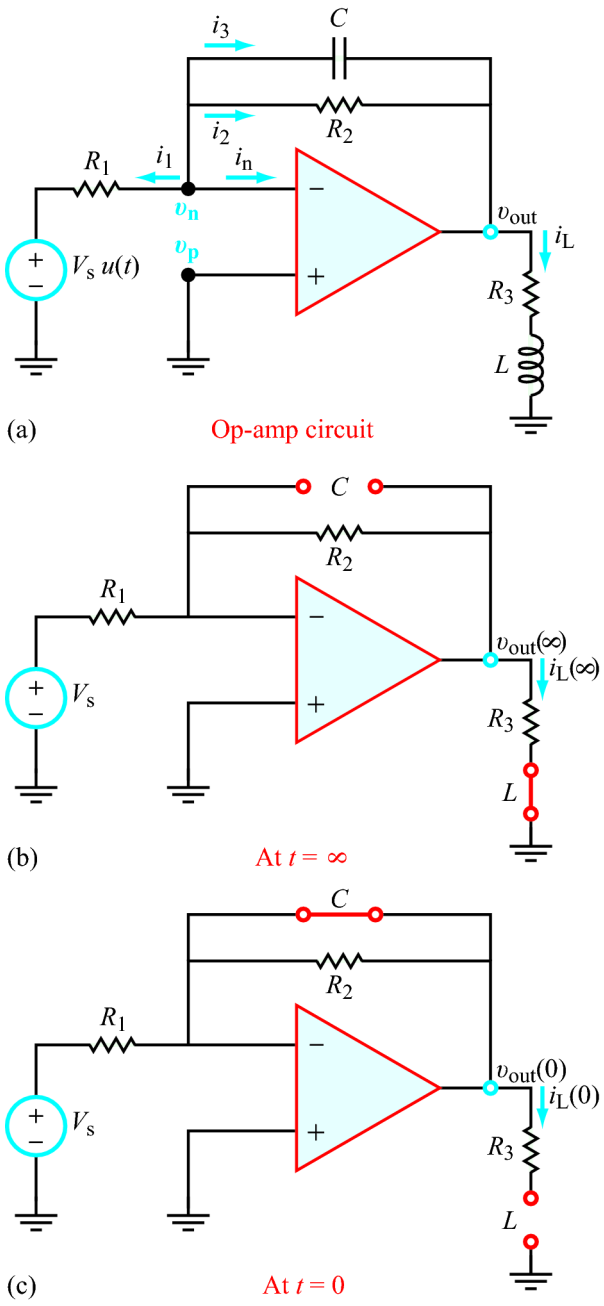


Figure 6.18 Op-amp circuit of Example 6-12.

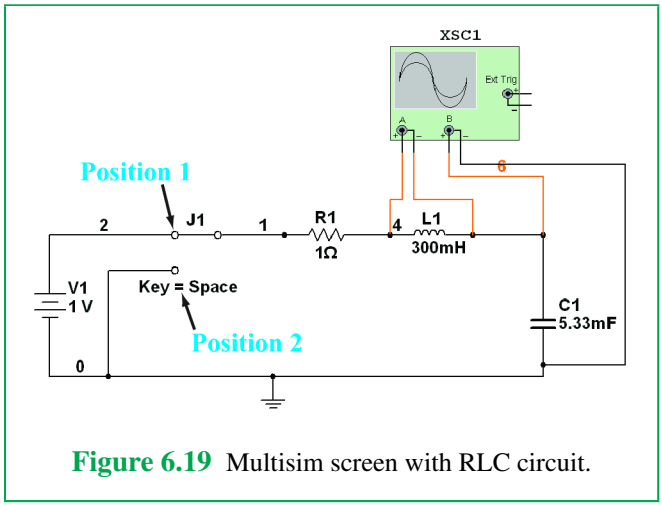


Figure 6.19 Multisim screen with RLC circuit.

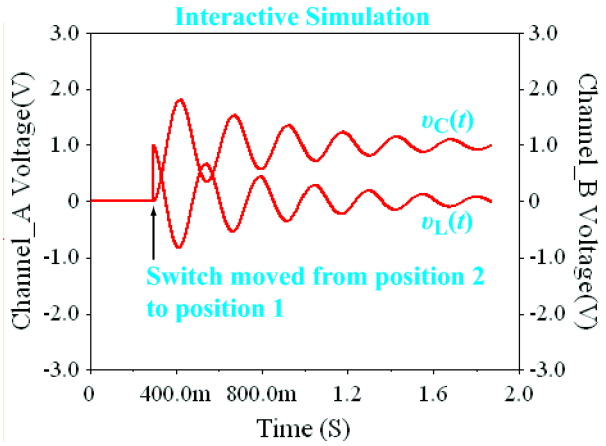


Figure 6.20 Voltage responses to moving the switch in the RLC circuit from position 2 to position 1.

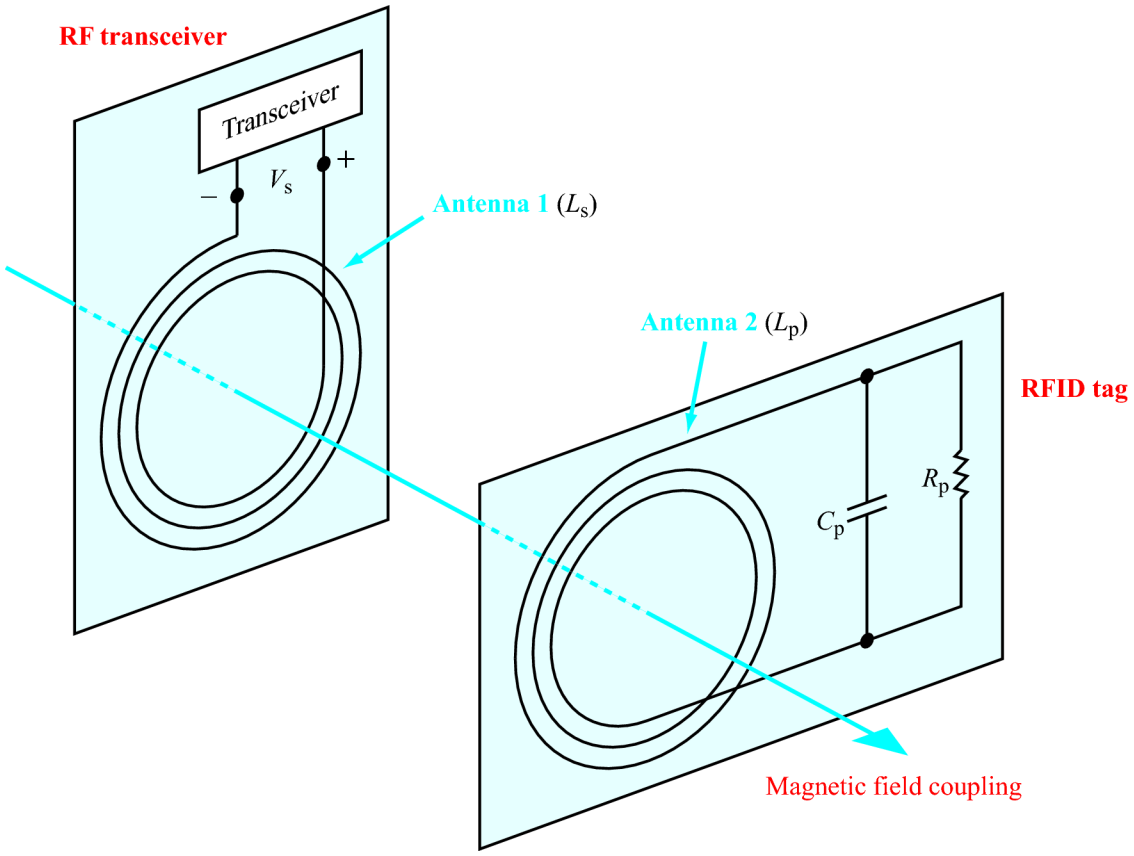


Figure 6.21 Illustration of an RFID transceiver in close proximity to an RFID tag. Note that the RFID tag will only couple to the transceiver when the two inductors are aligned along the magnetic field (shown in blue).

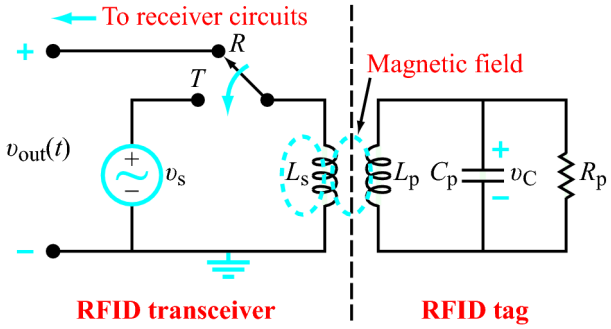


Figure 6.22 Basic elements of the RFID.

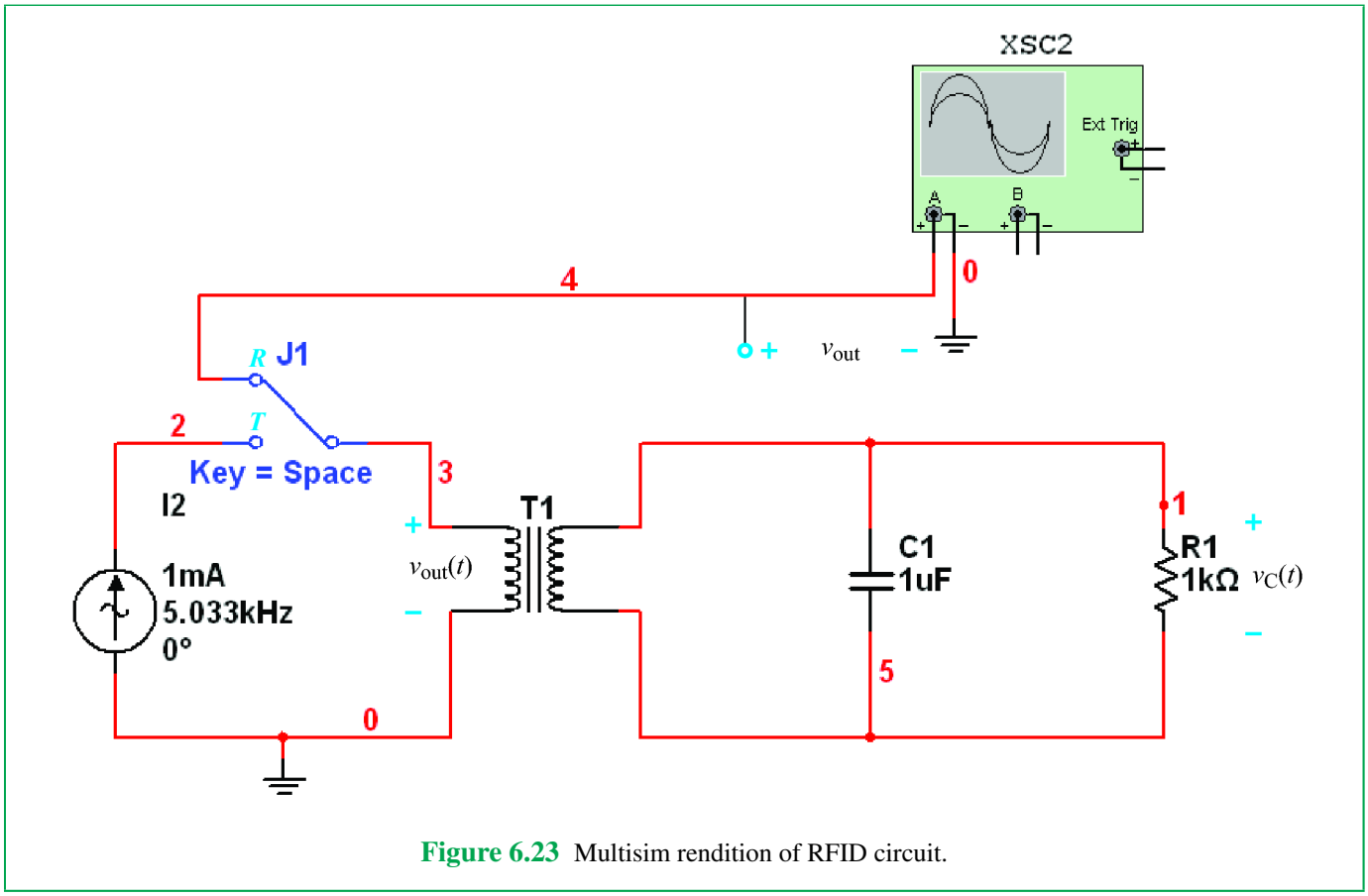


Figure 6.23 Multisim rendition of RFID circuit.

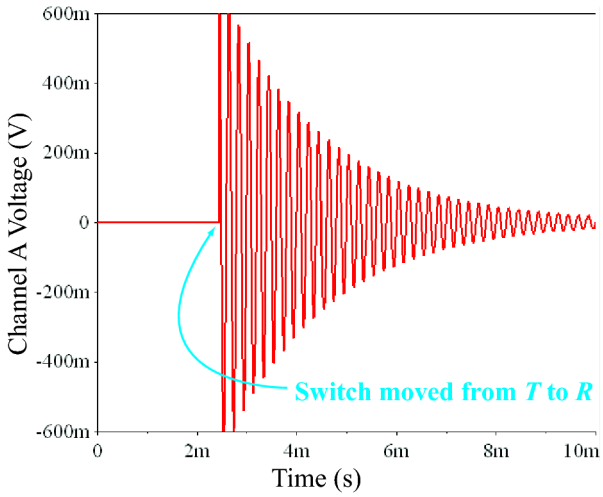


Figure 6.24 Oscilloscope trace for RFID receive channel $v_{out}(t)$ after moving the switch from T to R.

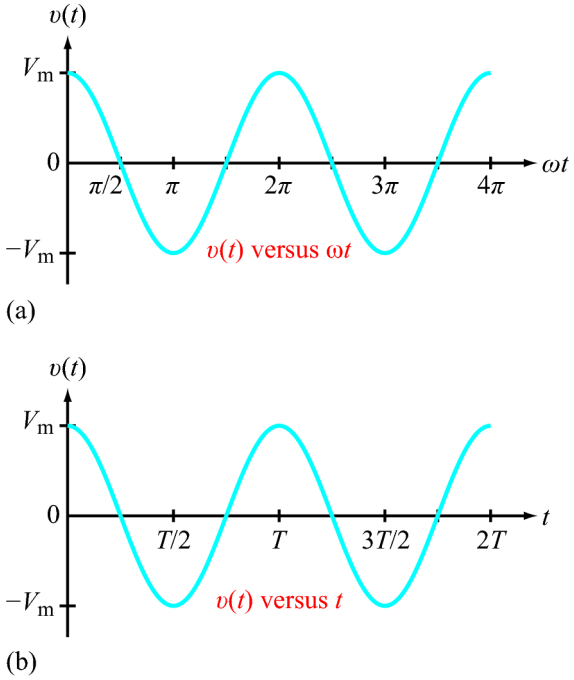


Figure 7.1 The function $v(t) = V_m \cos \omega t$ plotted as a function of (a) ωt and (b) t.

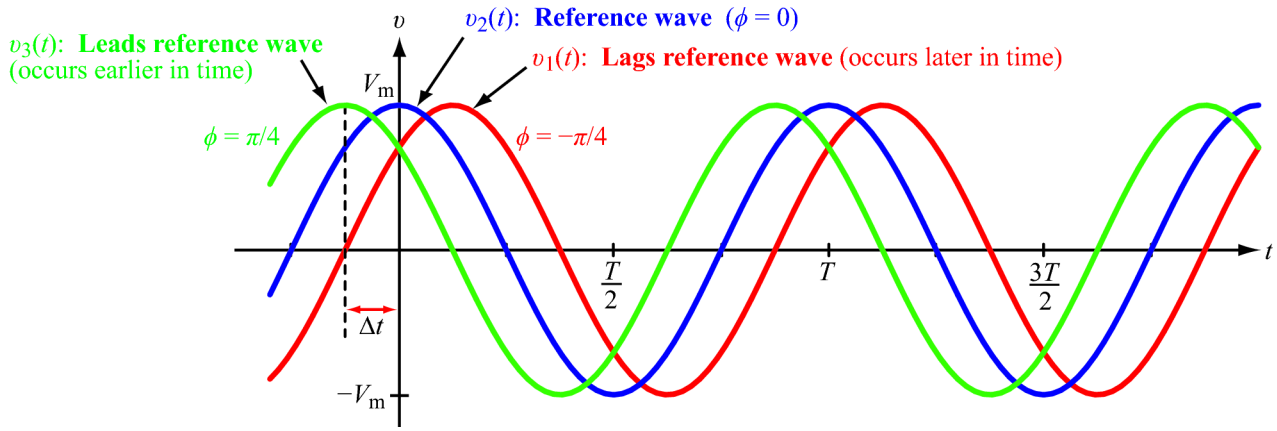


Figure 7.2 Plots of $v(t) = V_m \cos[(2\pi t/T) + \phi]$ for three different values of ϕ.

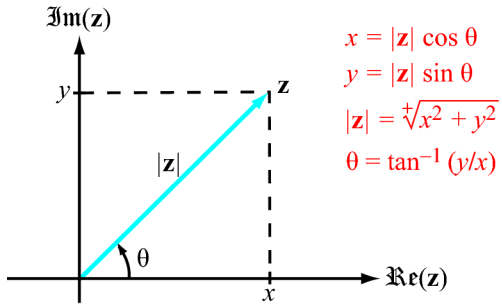


Figure 7.3 Relation between rectangular and polar representations of a complex number $\mathbf{z} = x + jy = |\mathbf{z}|e^{j\theta}$.

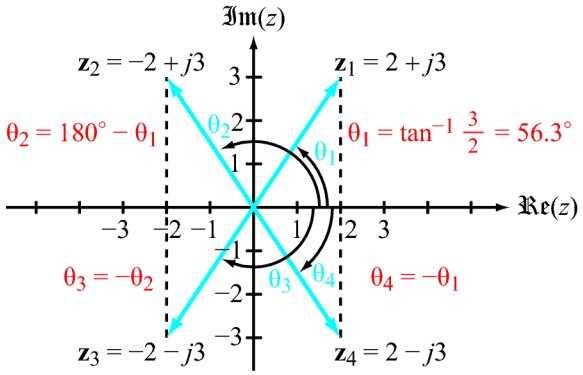


Figure 7.4 Complex numbers $\mathbf{z}_1$ to $\mathbf{z}_4$ have the same magnitude $|\mathbf{z}| = \sqrt{2^2+3^2} = 3.61$, but their polar angles depend on the polarities of their real and imaginary components.

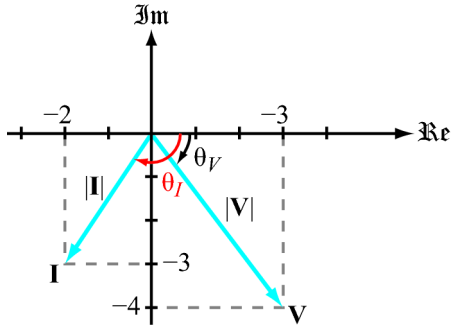


Figure 7.5 Complex numbers **V** and **I** in the complex plane (Example 7-3).

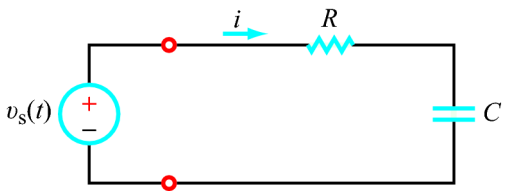


Figure 7.6 RC circuit connected to an ac source.

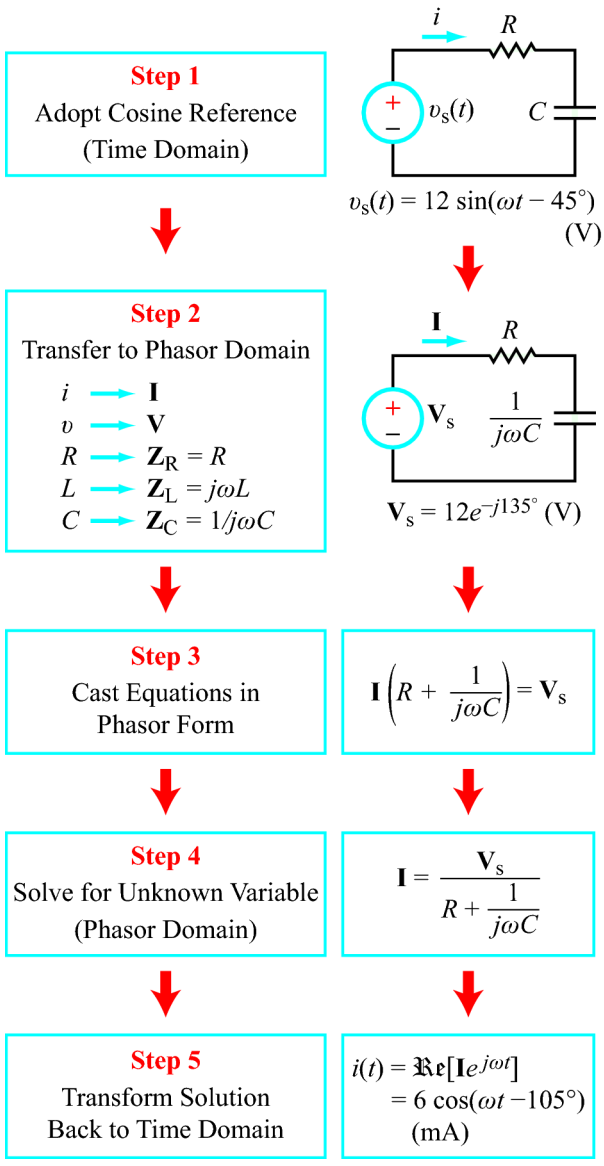


Figure 7.7 Five-step procedure for analyzing ac circuits using the phasor-domain technique.

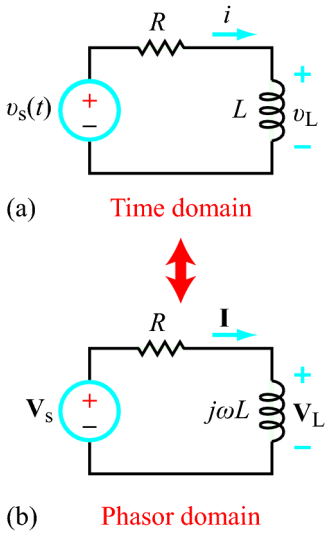


Figure 7.8 RL circuit of Example 7-5.

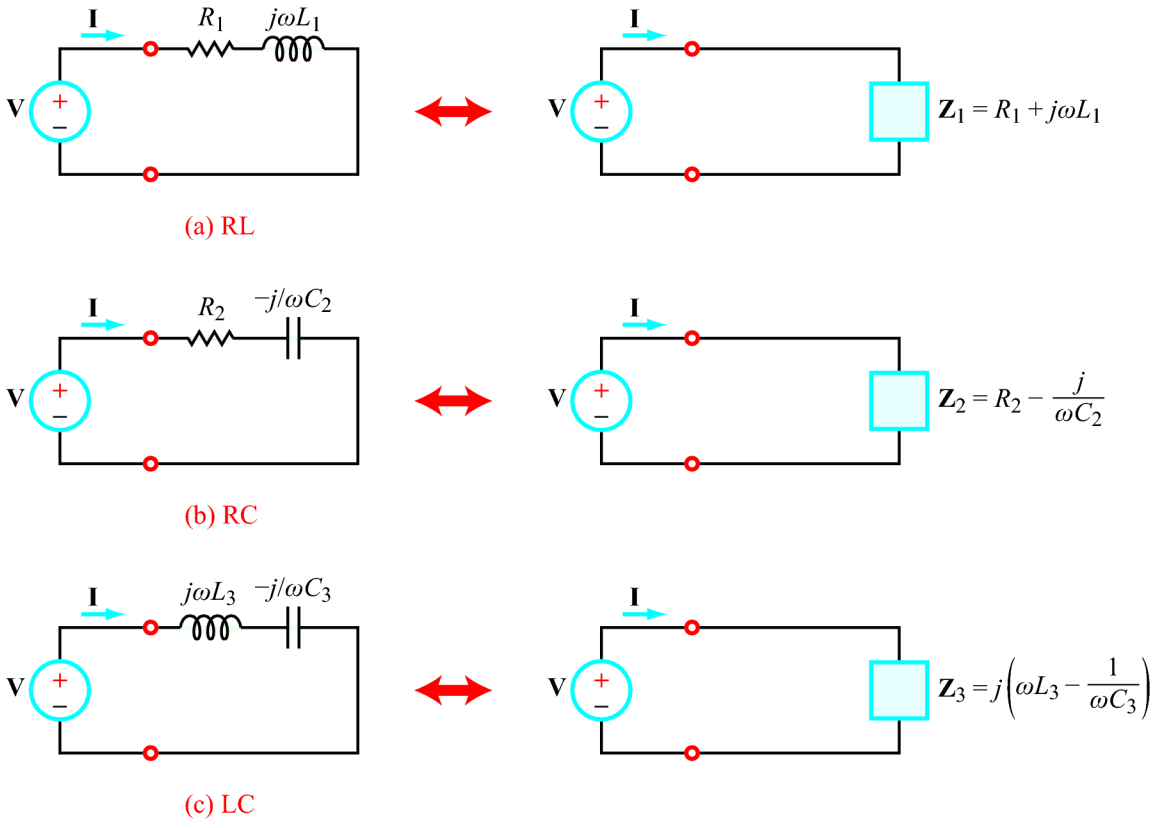


Figure 7.9 Three different, two-element, series combinations.

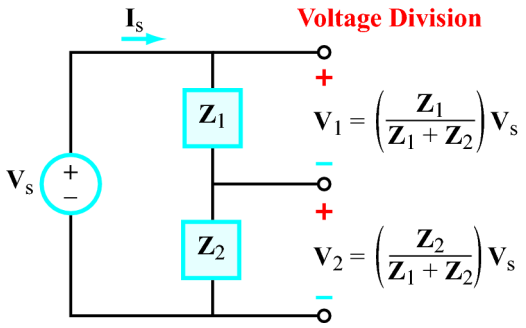


Figure 7.10 Voltage division among two impedances in series.

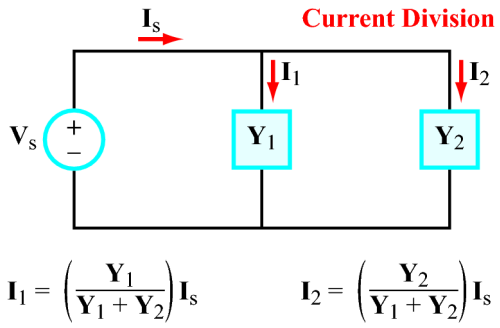


Figure 7.11 Current division among two admittances in parallel.

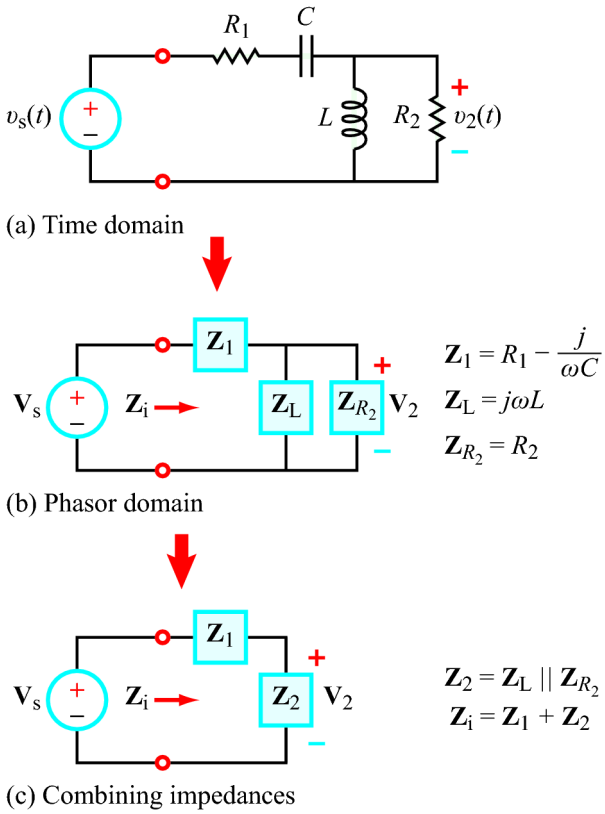


Figure 7.12 Circuit for Example 7-6.

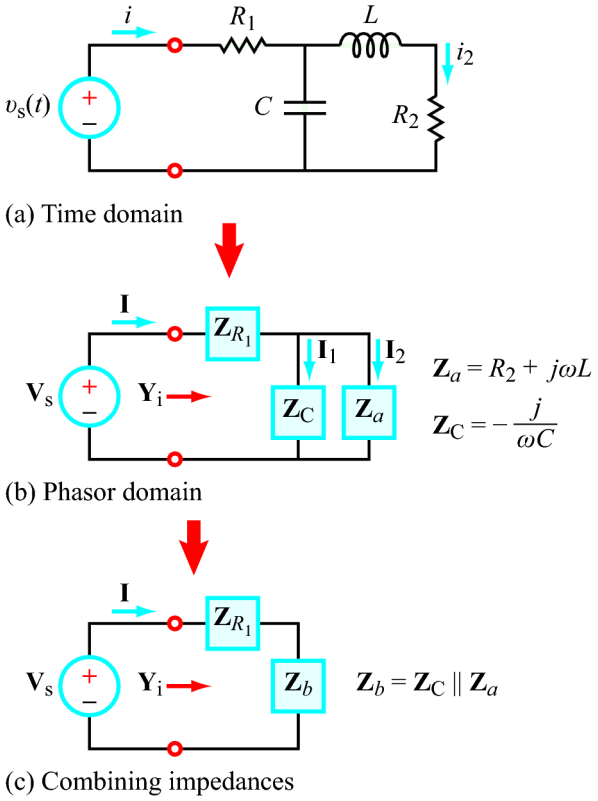
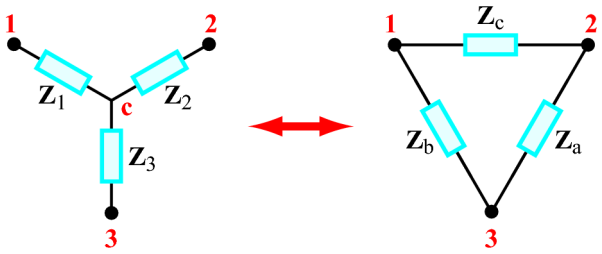


Figure 7.13 Circuit for Example 7-7.



(a) Y circuit (b) Δ circuit

Figure 7.14 Y–Δ equivalent circuits.

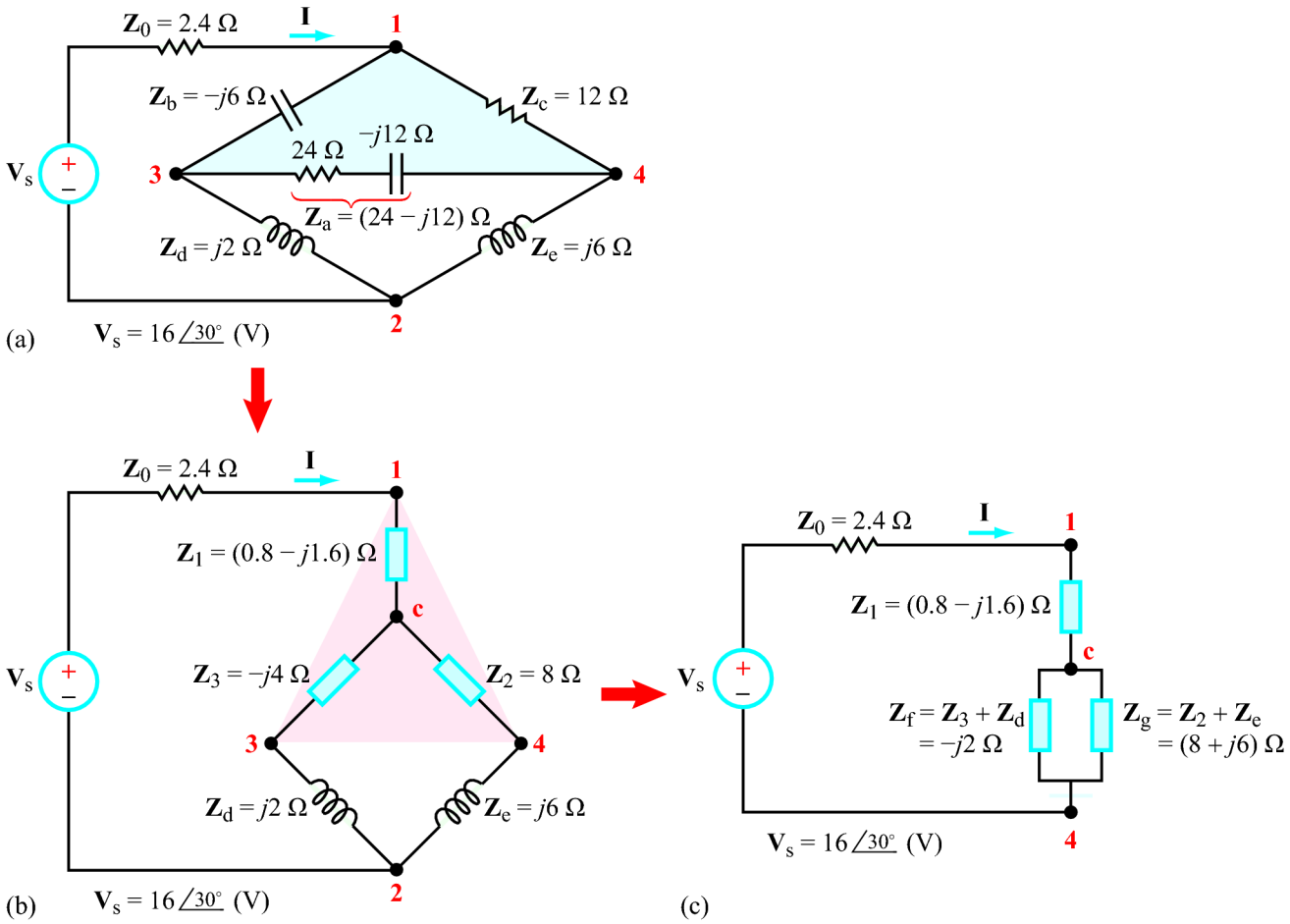


Figure 7.15 Example 7-8 circuit evolution.

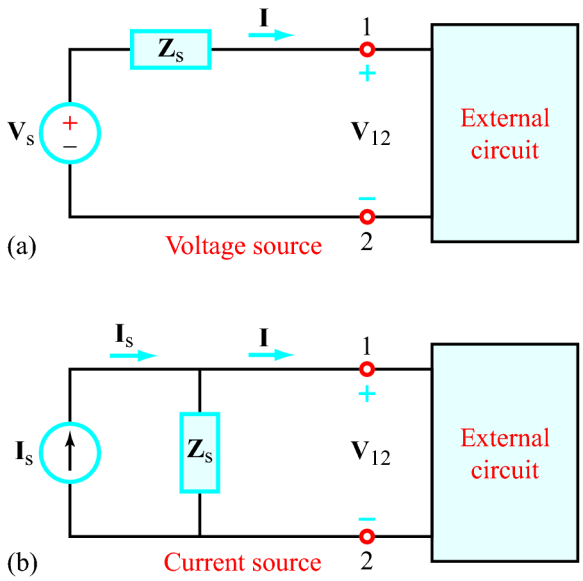


Figure 7.16 Source-transformation equivalency.

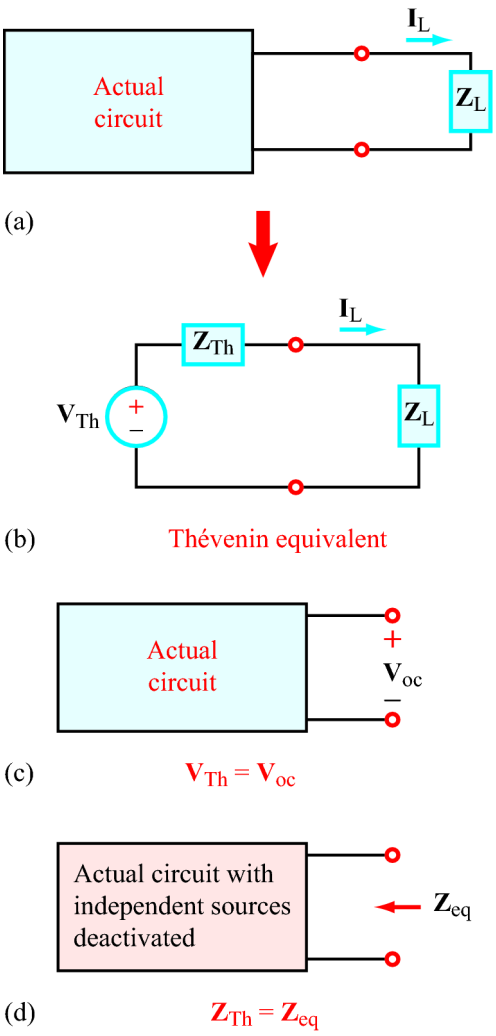


Figure 7.17 Thévenin-equivalent method for a circuit with no dependent sources.

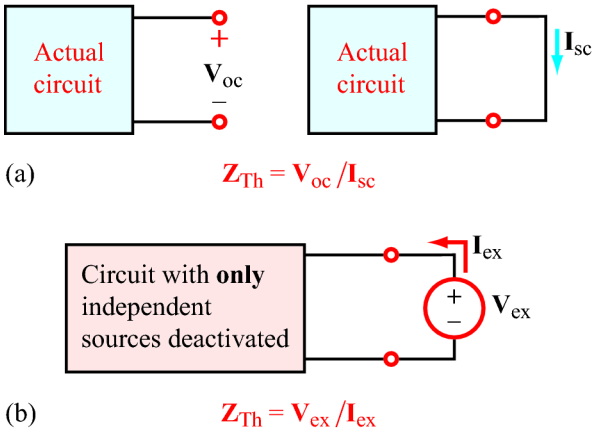


Figure 7.18 The (a) open-circuit/short-circuit method and (b) the external-source method are both suitable for determining $\mathbf{Z}_{Th}$, whether or not the circuit contains dependent sources.

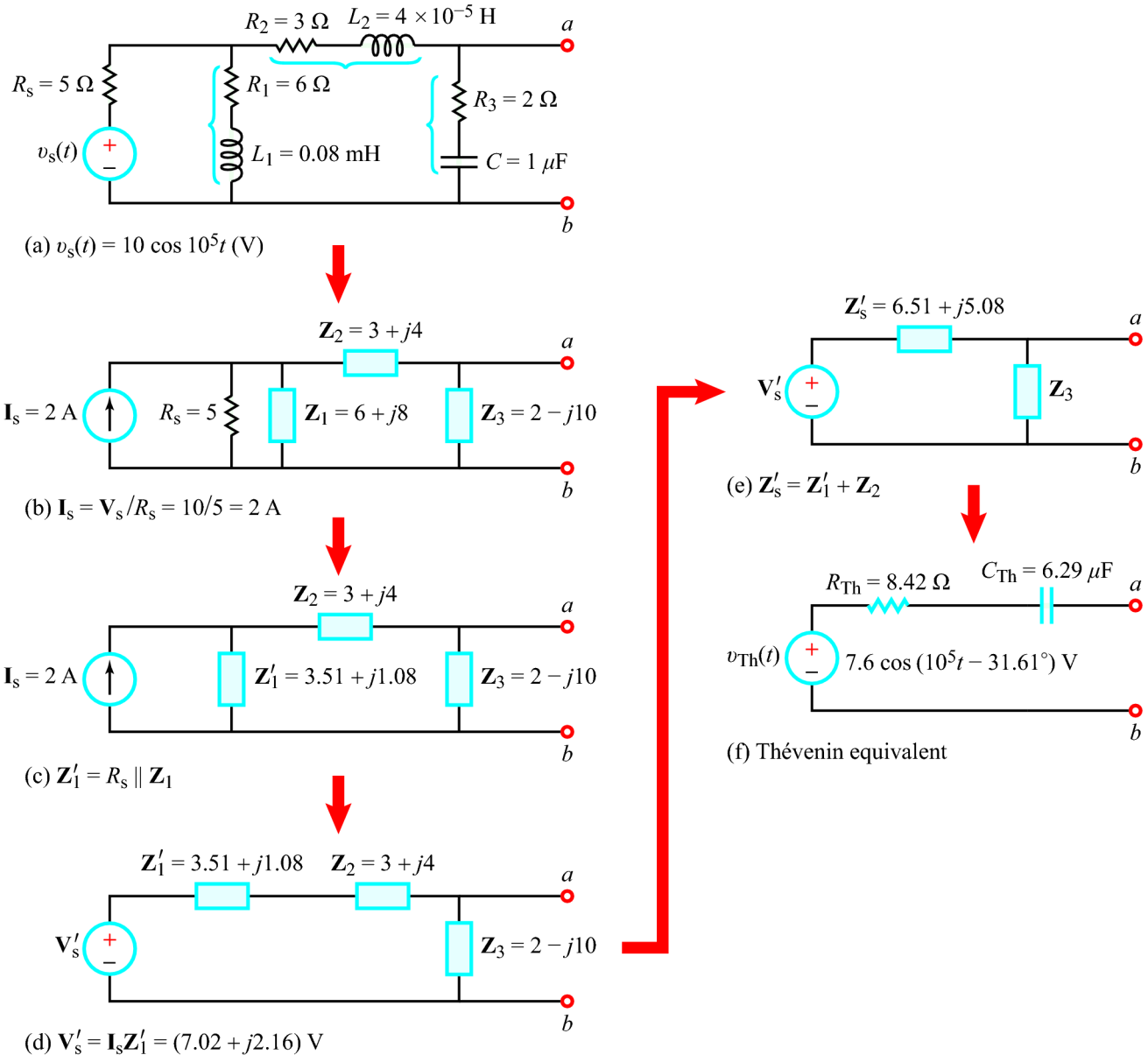


Figure 7.19 Using source transformation to simplify the circuit of Example 7-9. (All impedances are in ohms.)

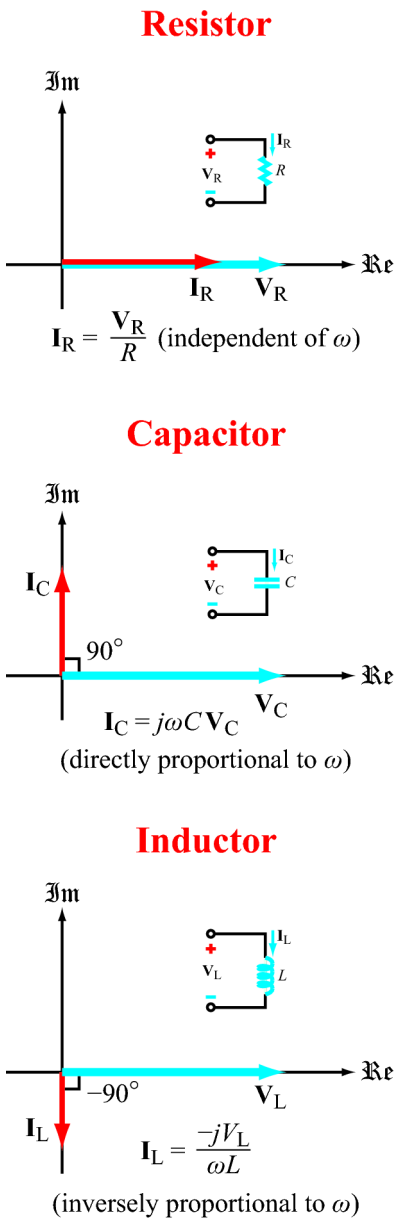


Figure 7.20 Phasor diagrams for R, L, and C.

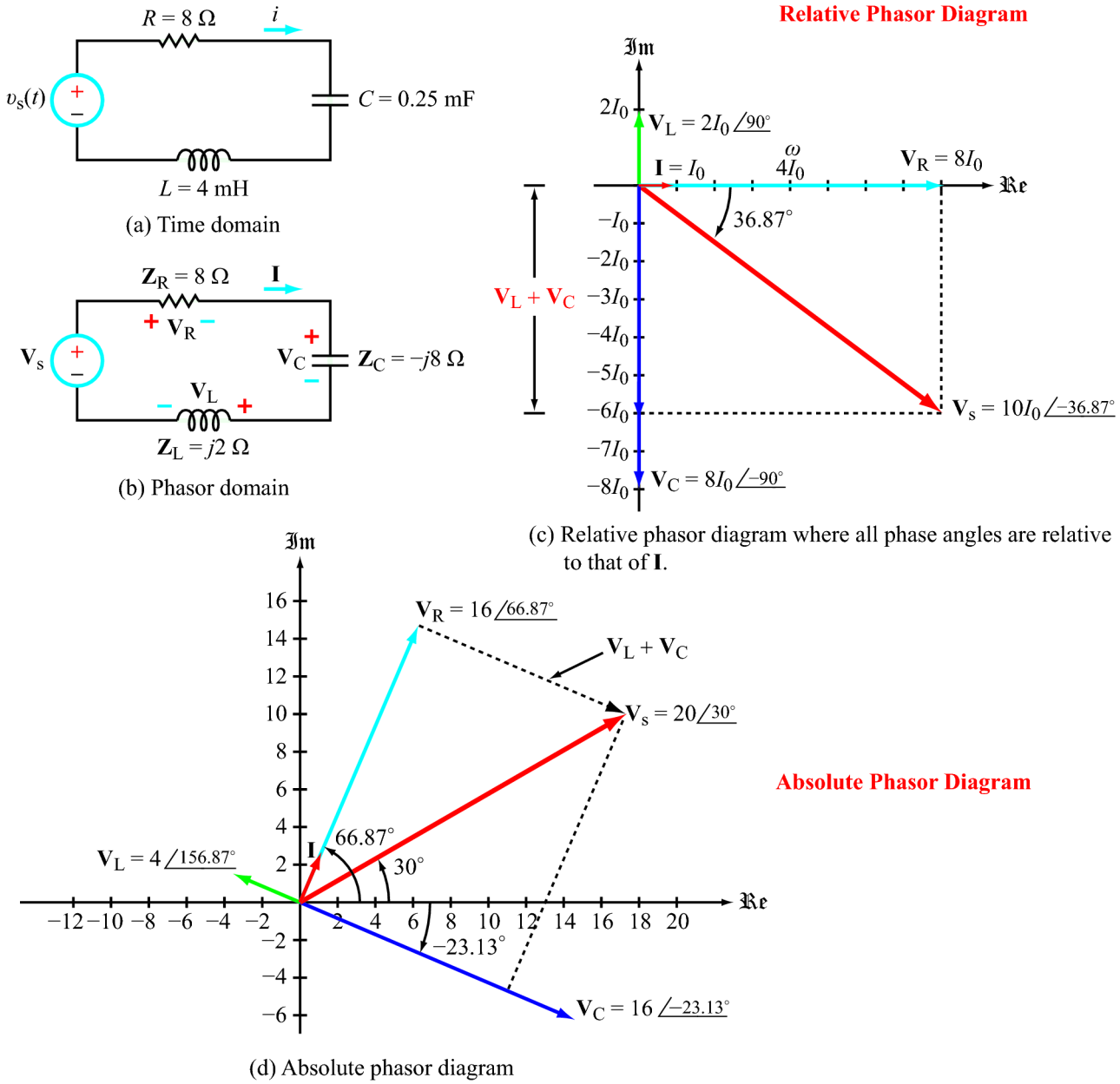


Figure 7.21 Circuit and phasor diagrams for Example 7-10. The true phase angle of $\mathbf{I}$ is 66.87°, so if the relative phasor diagram in (c) were to be rotated counterclockwise by that angle and the scale adjusted to incorporate the fact $I_0 = 2$, the diagram would coincide with the absolute phasor diagram in (d).

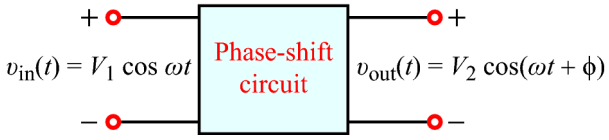
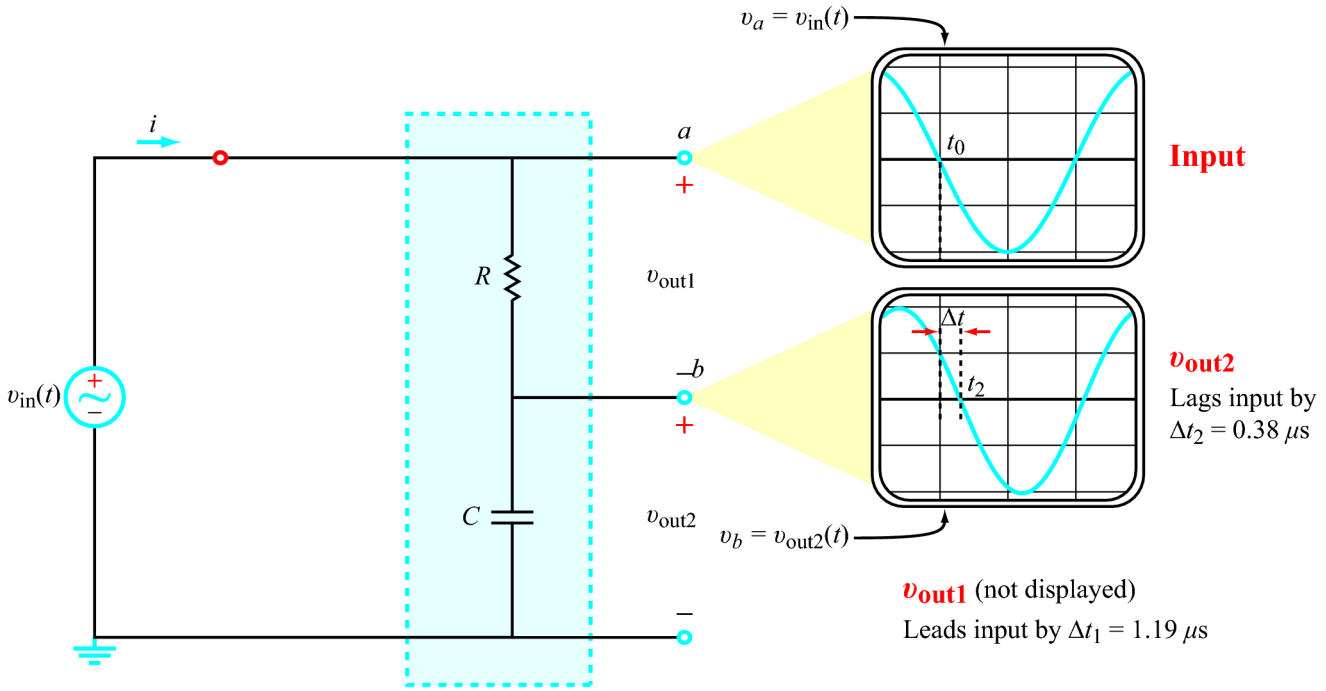
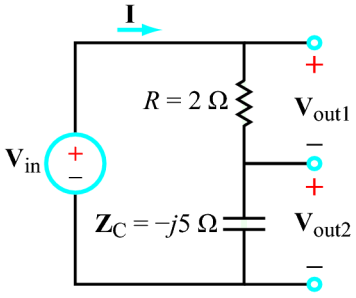


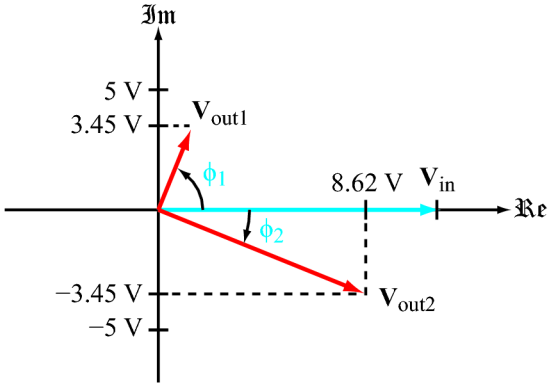
Figure 7.22 The phase-shift circuit changes the phase of the input signal by ϕ.



(a) Time-domain waveforms



(b) Phasor-domain circuit



(c) Phasors $\mathbf{V}_{in}$, $\mathbf{V}_{out1}$, and $\mathbf{V}_{out2}$ in the complex plane

Figure 7.23 RC phase-shift circuit: the phase of v_{out1} (across R) leads the phase of $v_{in}(t)$, whereas the phase of v_{out2} (across C) lags the phase of $v_{in}(t)$.

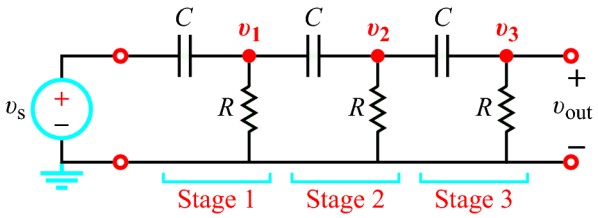


Figure 7.24 Three-stage, cascaded, RC phase-shifter (Example 7-11).

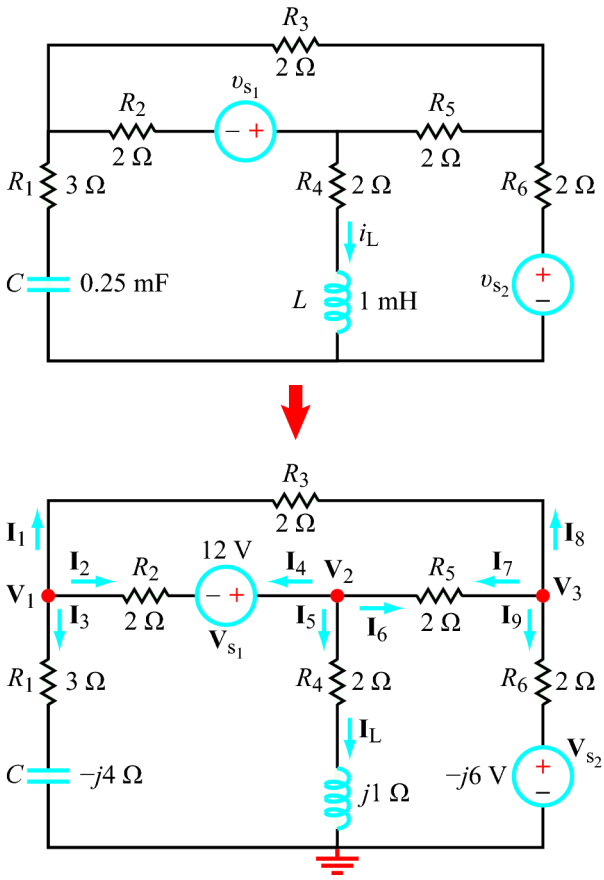


Figure 7.25 Circuit for Example 7-12 in (a) the time domain and (b) the phasor domain.

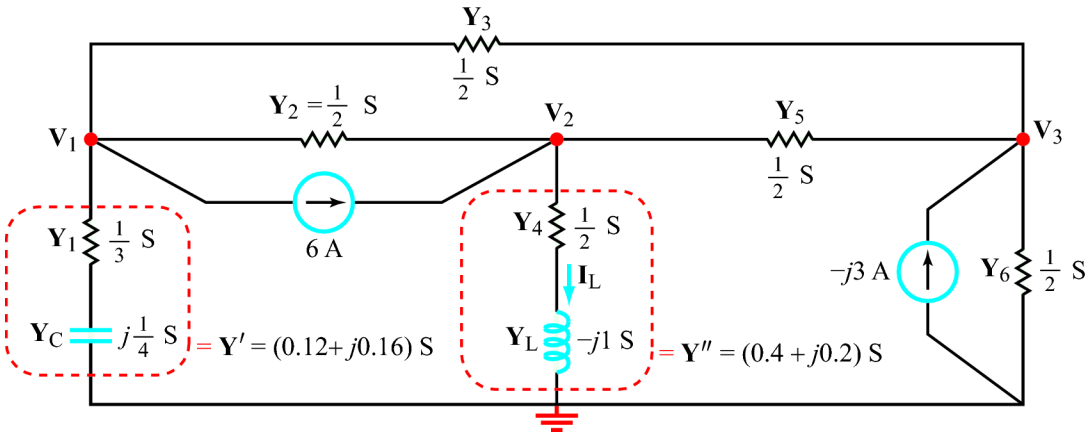


Figure 7.26 Equivalent of the circuit in **Fig.** 7.25, after source transformation of voltage sources into current sources and replacement of passive elements with their equivalent admittances.

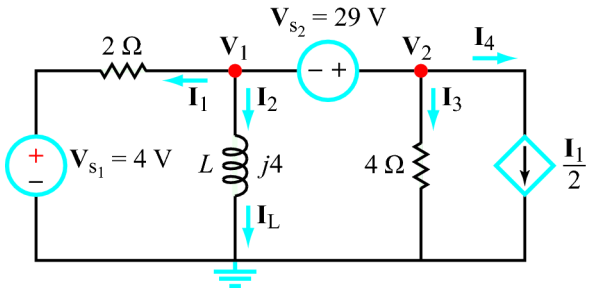


Figure 7.27 Phasor-domain circuit containing a supernode and a dependent source (Example 7-13).

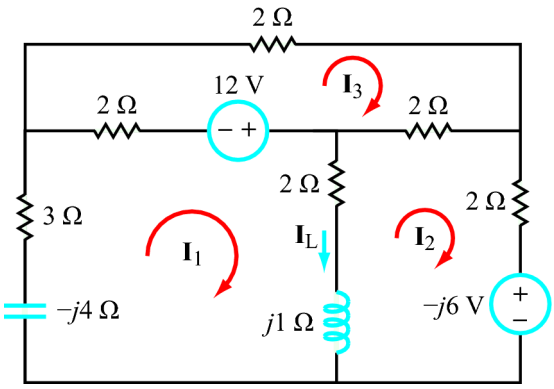


Figure 7.28 Circuit for Example 7-14.

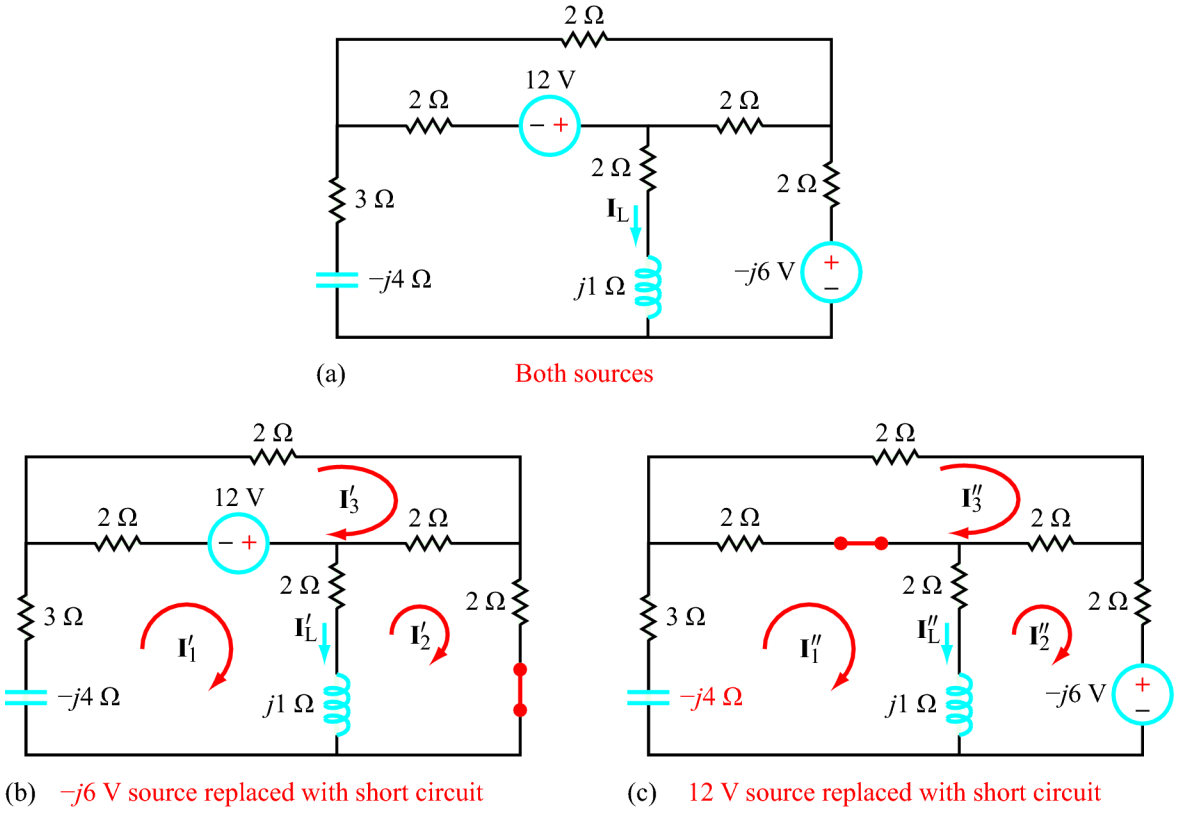
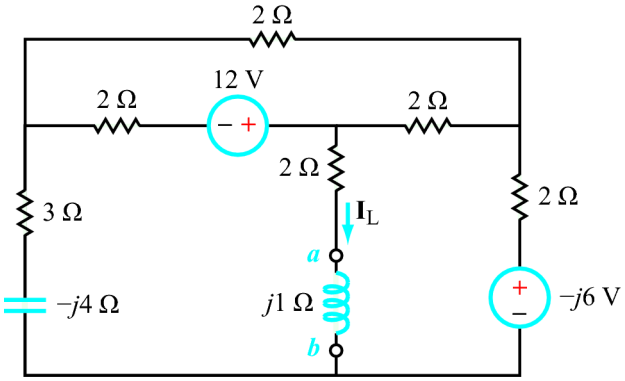
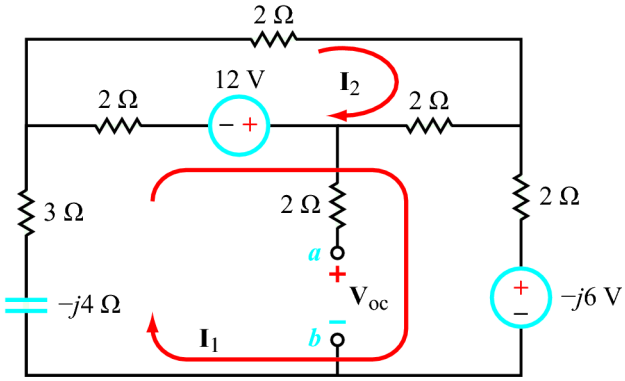


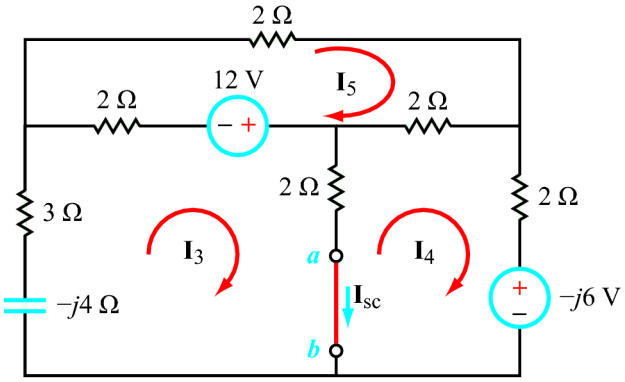
Figure 7.29 Demonstration of the source-superposition technique (Example 7-15).



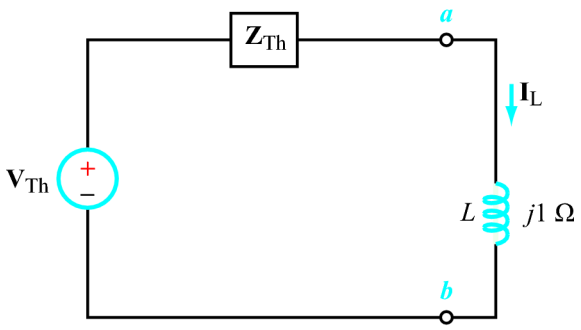
(a) Original circuit



(b) Inductor replaced with open circuit

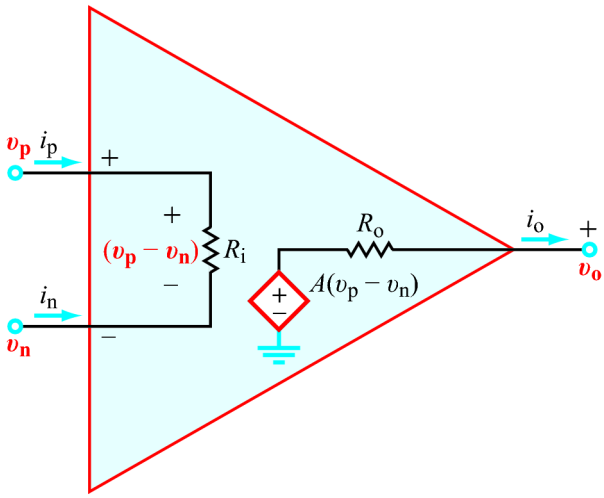


(c) Inductor replaced with short circuit

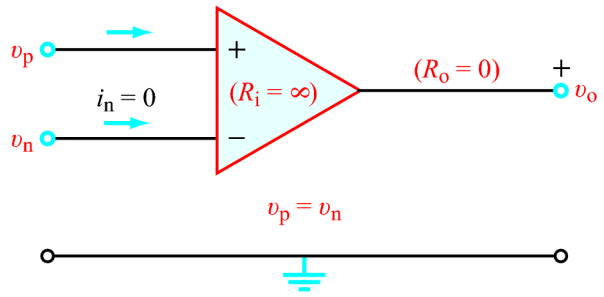


(d) Thévenin circuit connected to inductor

Figure 7.30 After determining the open-circuit voltage in part (b) and the short-circuit current in part (c), the Thévenin equivalent circuit is connected to the inductor to determine $\mathbf{I}_L$.



(a) Op-amp equivalent circuit



(b) Ideal op-amp model

Figure 7.31 Op-amp (a) equivalent circuit (for both dc and ac) and (b) ideal model (for dc, and ac at low frequencies).

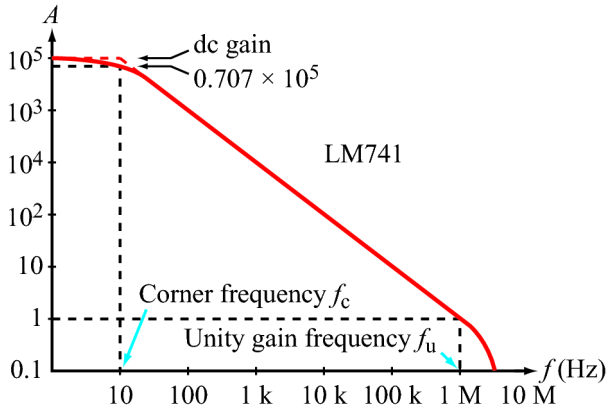
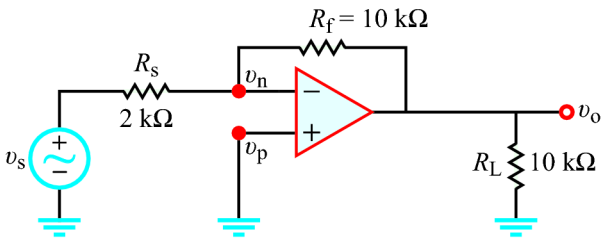
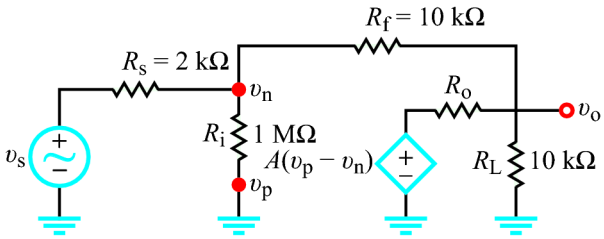


Figure 7.32 Open-loop gain A versus frequency for the LM741 op amp.



(a) Inverting amplifier circuit



(b) Equivalent circuit model

Figure 7.33 Inverting amplifier.

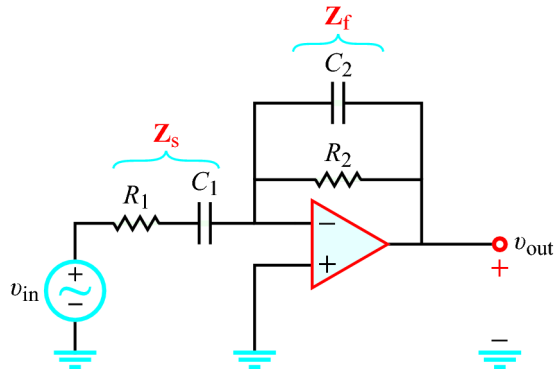


Figure 7.34 Inverting amplifier as a phase-shift circuit.

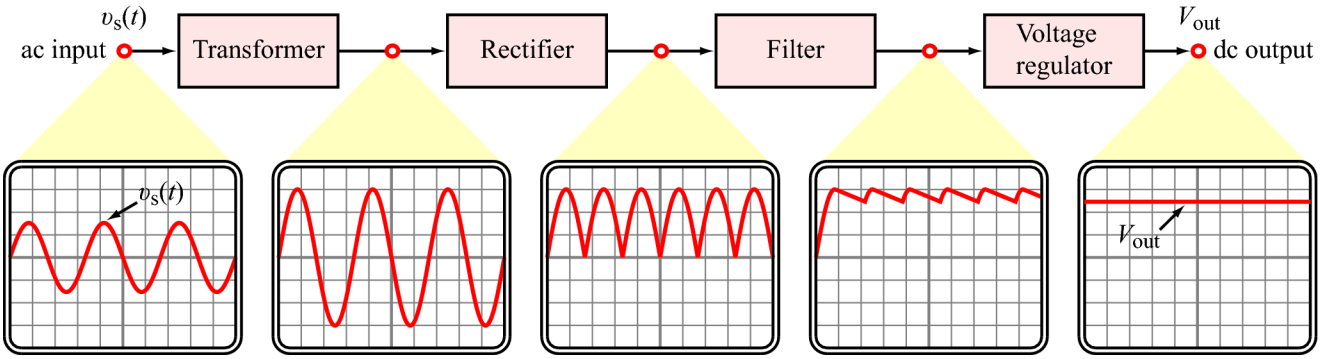


Figure 7.35 Block diagram of a basic dc power supply.

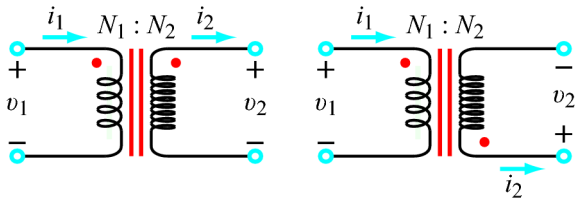


Figure 7.36 Schematic symbol for an ideal transformer. Note the reversal of the voltage polarity and current direction when the dot location at the secondary is moved from the top end of the coil to the bottom end. For both configurations:

$$\frac{v_2}{v_1} = \frac{N_2}{N_1} = n, \qquad \frac{i_2}{i_1} = \frac{N_1}{N_2} = \frac{1}{n}, \qquad \frac{p_2}{p_1} = \frac{v_2 i_2}{v_1 i_1} = 1$$

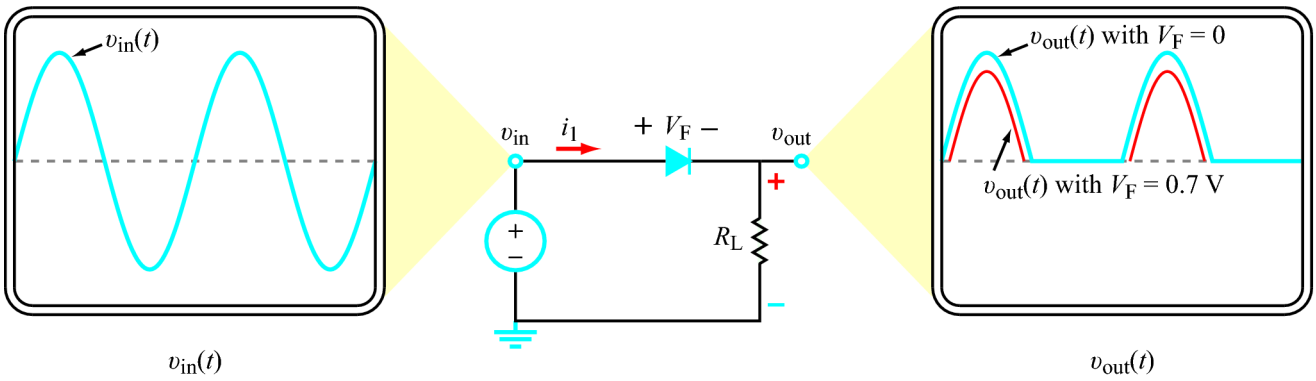


Figure 7.37 Half-wave rectifier circuit.

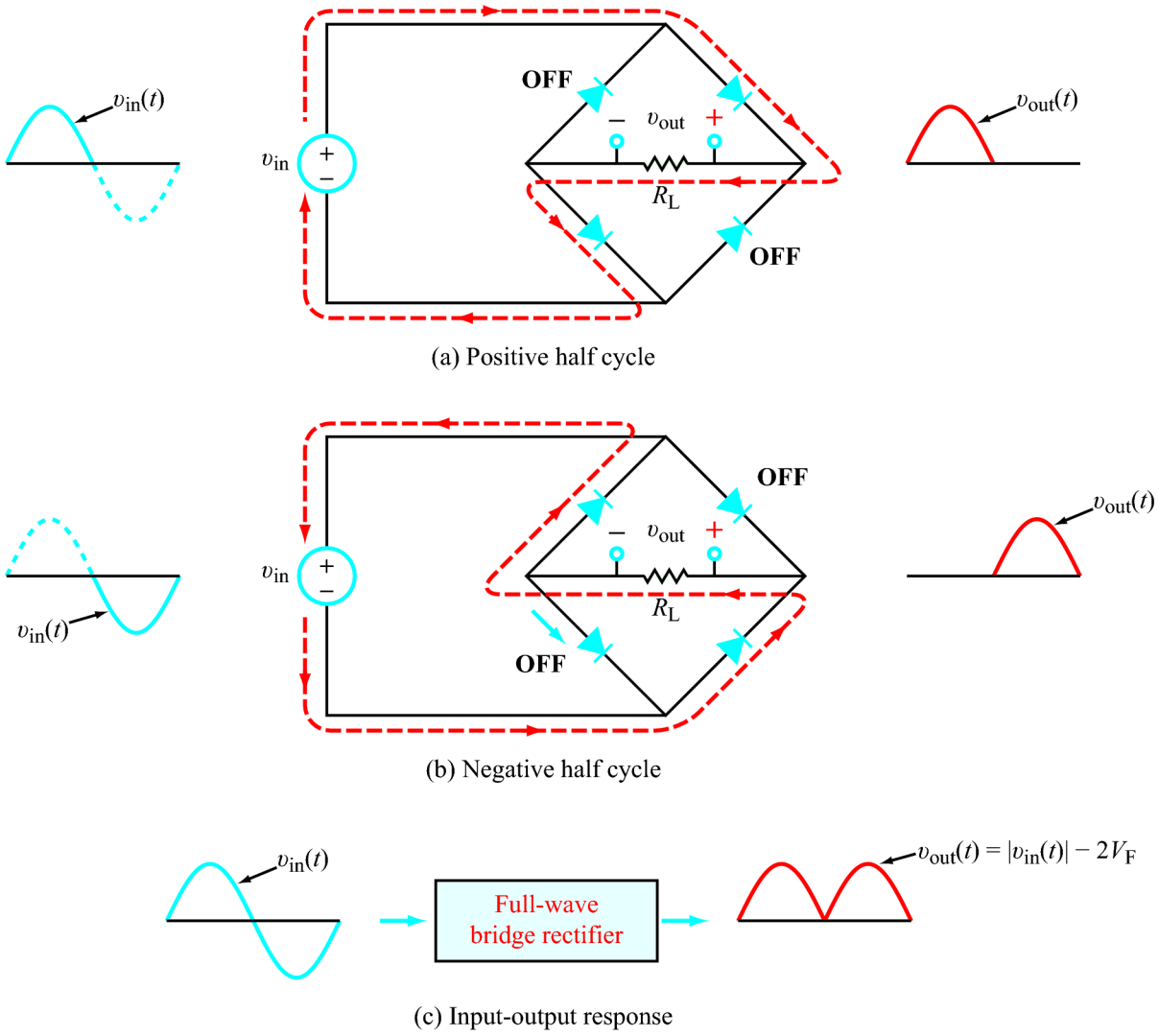
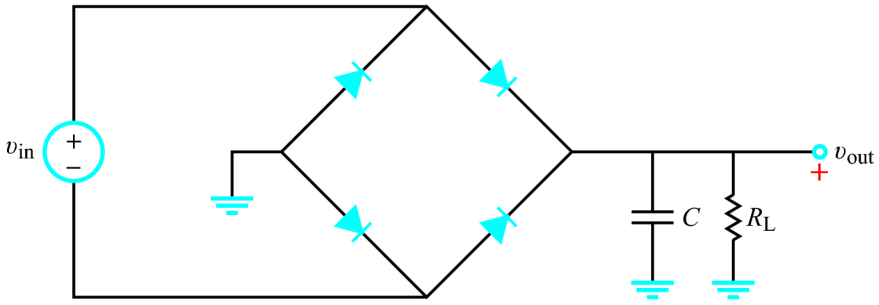
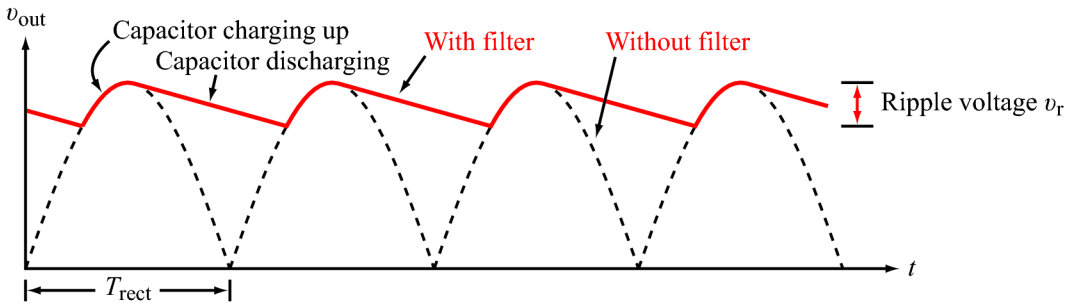


Figure 7.38 Full-wave bridge rectifier. Current flows in the same direction through the load resistor for both half cycles.



(a) Bridge rectifier with filter



(b) Filtered output

Figure 7.39 Smoothing filter reduces the variations of waveform $v_{out}(t)$.

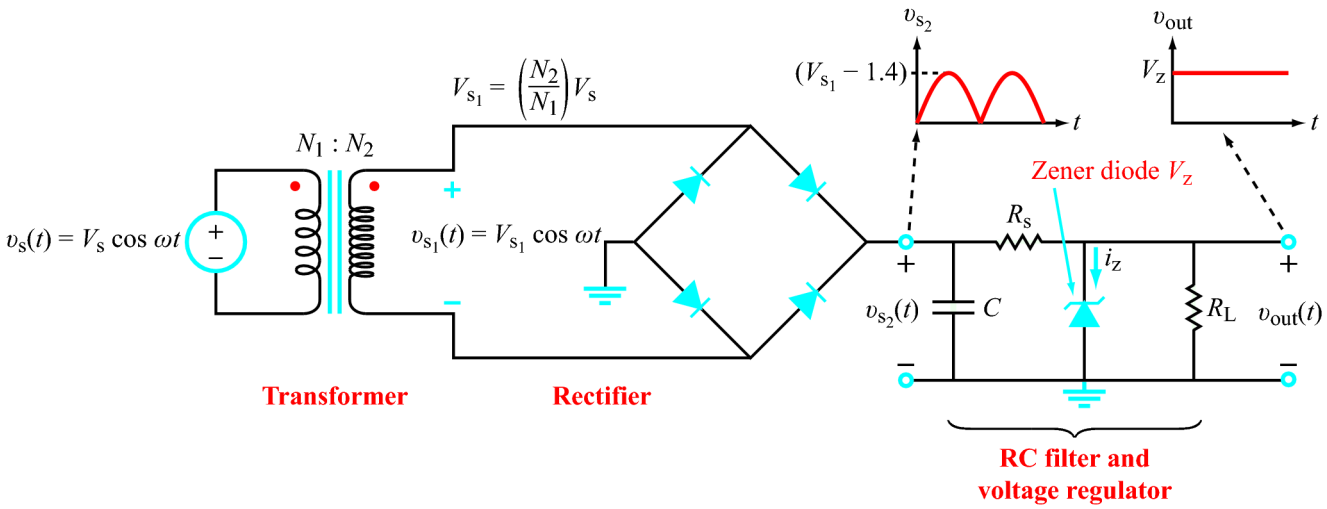


Figure 7.40 Complete power-supply circuit.

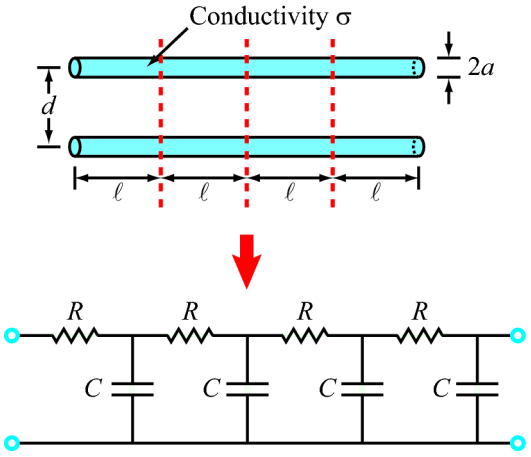


Figure 7.41 Distributed impedance model of two-wire transmission line.

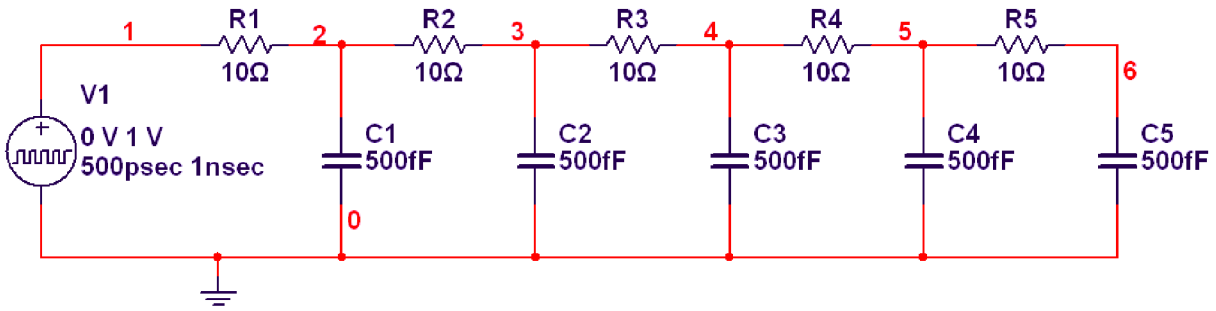


Figure 7.42 Transmission-line circuit in Multisim.

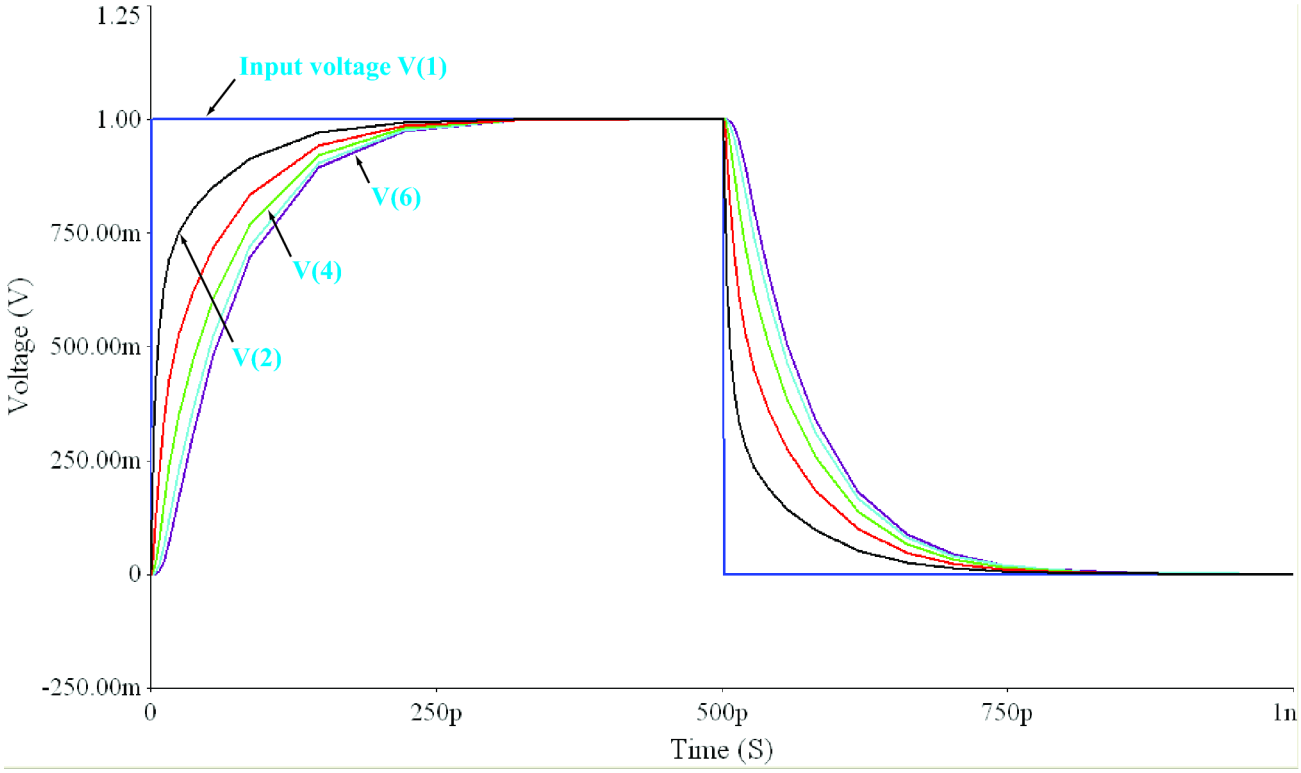


Figure 7.43 Multisim display of voltage waveforms at nodes 1, 2, 3, 4, 5, and 6.

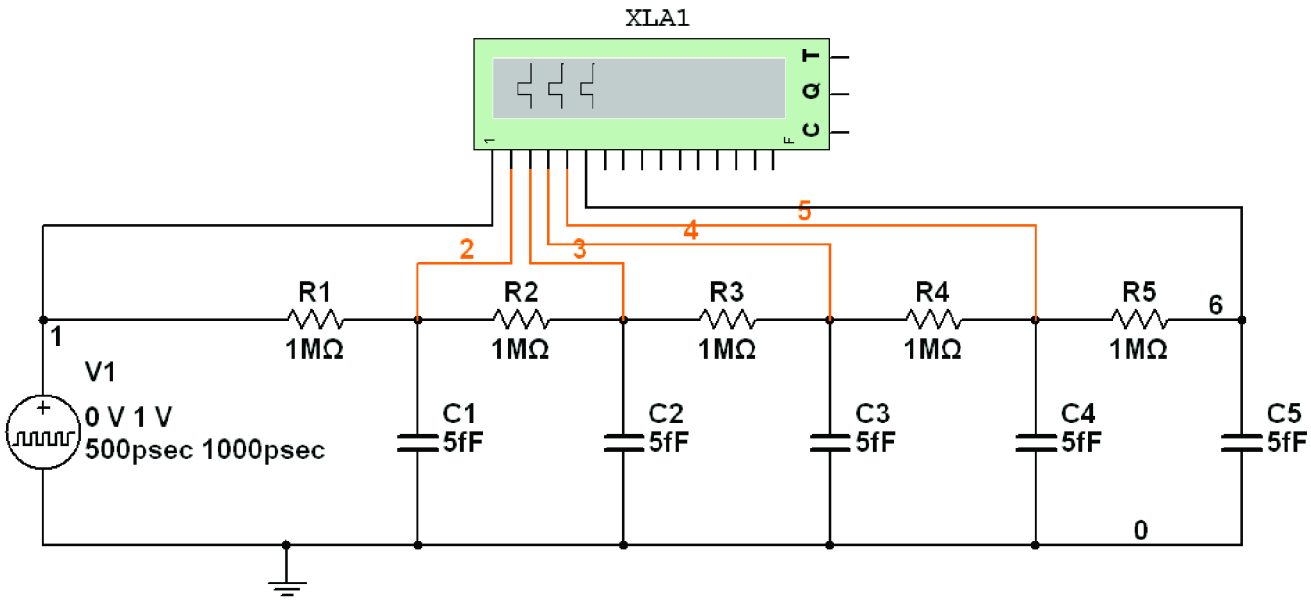


Figure 7.44 Using the Logic Analyzer to measure time delay in Multisim.

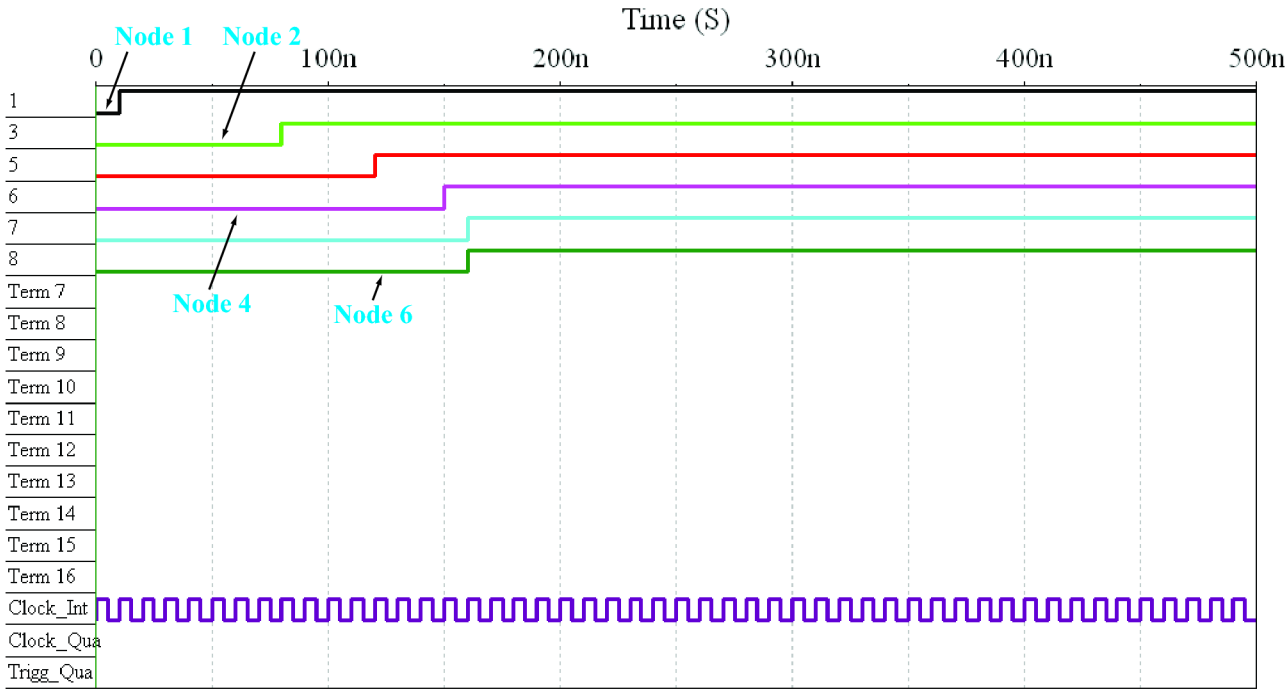


Figure 7.45 Logic Analyzer readout at nodes 1, 2, 3, 4, 5, and 6.

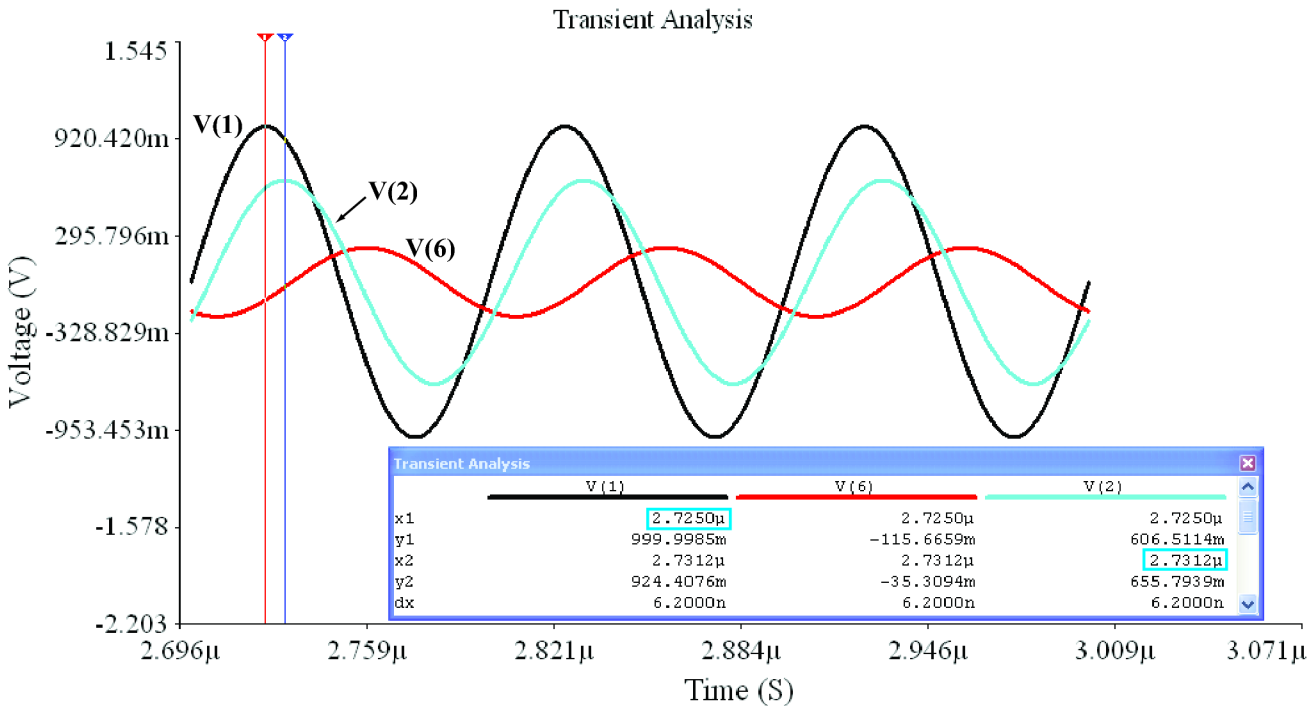


Figure 7.46 Multisim Grapher Plot of voltage nodes V(1), V(2), and V(6) in the circuit of **Fig.** 7.42.

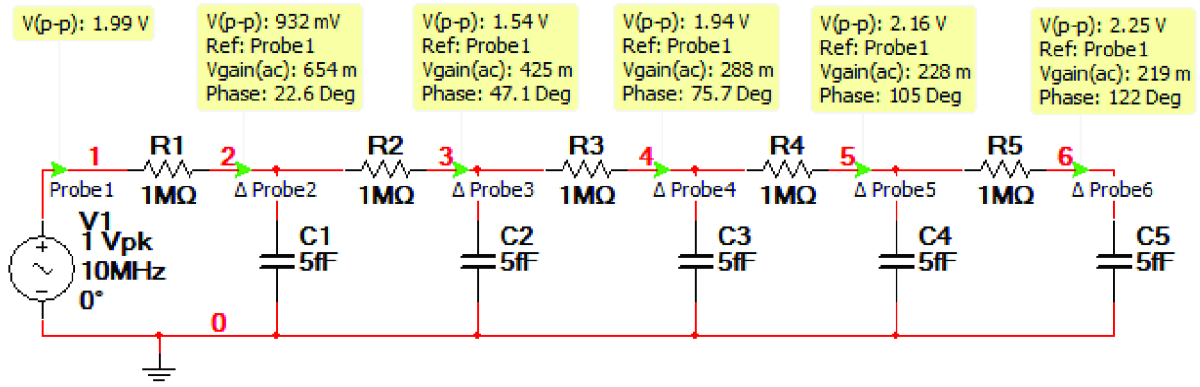


Figure 7.47 Using Measurement Probes to determine phase and amplitude of signal at various points on transmission line.

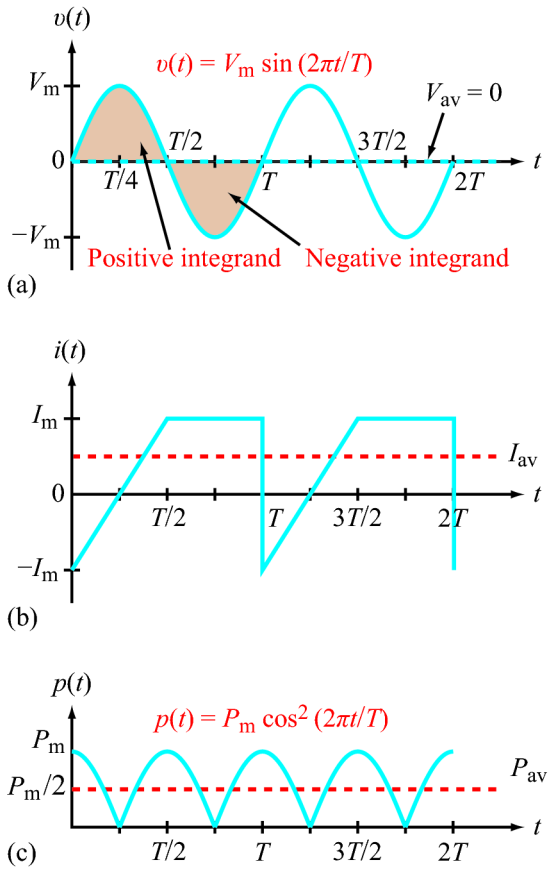


Figure 8.1 Examples of three periodic waveforms.

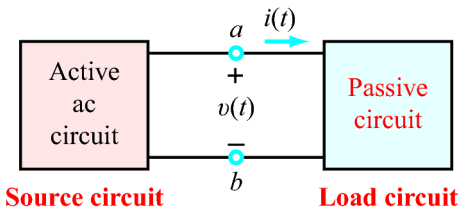


Figure 8.2 Passive load circuit connected to an input source at terminals (a, b).

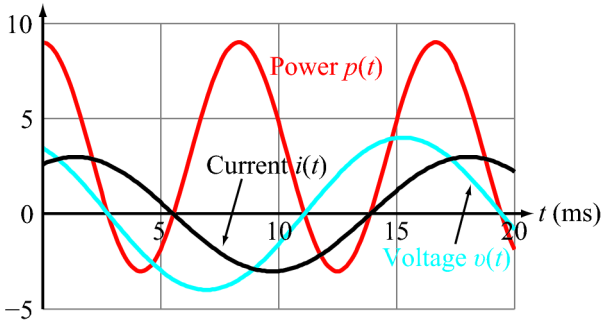


Figure 8.3 Waveforms for a 60 Hz circuit with $v(t) = 4\cos(377t + 30°)$ V, $i(t) = 3\cos(377t - 30°)$ A, and $p(t) = v(t)\, i(t)$. The waveform of $i(t)$ is shifted by 60° behind that of $v(t)$, and the oscillation frequency of $p(t)$ is twice that of $v(t)$ or $i(t)$.

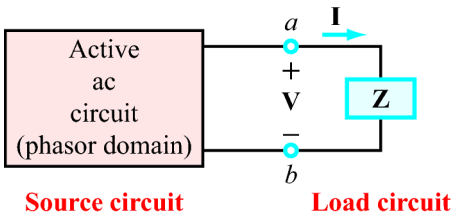
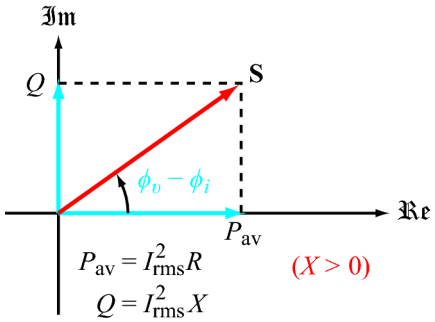
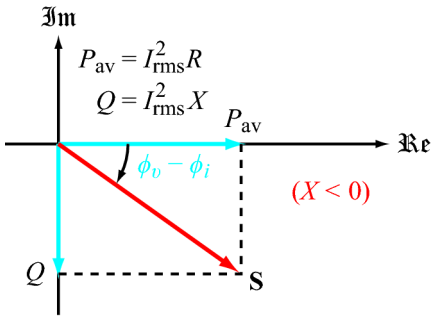


Figure 8.4 Source circuit connected to an impedance **Z** of a load circuit.

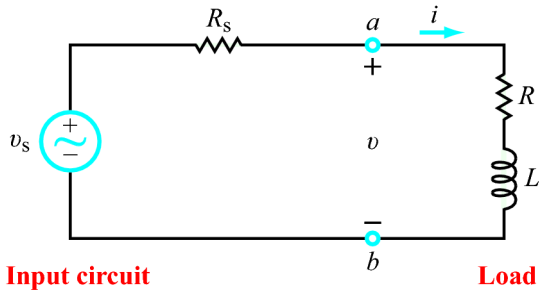


(a) Inductive load

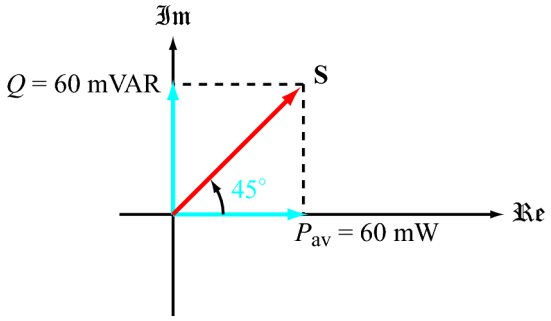


(b) Capacitive load

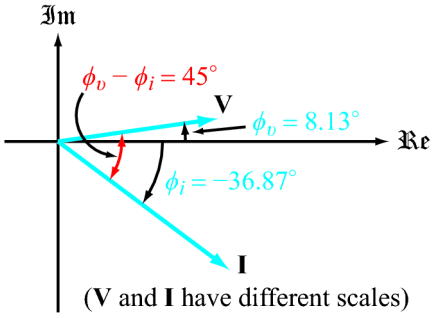
Figure 8.5 Complex power **S** lies in quadrant 1 for an inductive load and in quadrant 4 for a capacitive load.



(a) Circuit



(b) **S** in complex plane



(c) **V** and **I** in complex plane

Figure 8.6 Example 8-3.

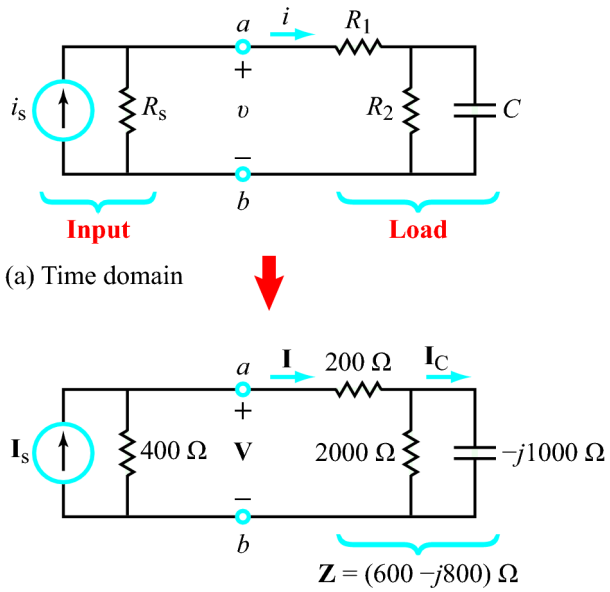
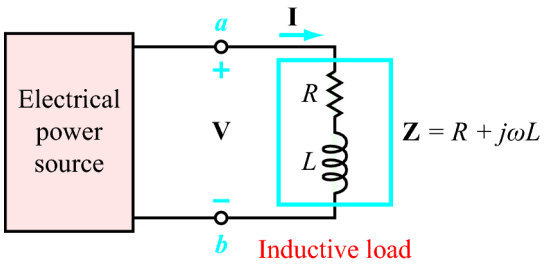
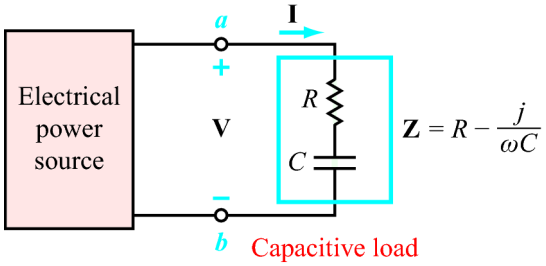


Figure 8.7 Circuit for Example 8-4.

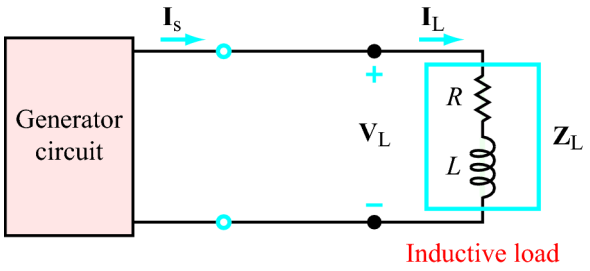


(a)

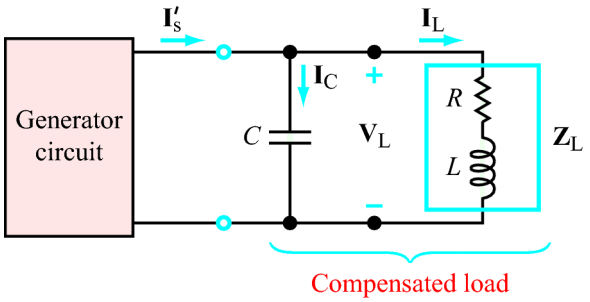


(b)

Figure 8.8 Inductive and capacitive loads connected to an electrical source.

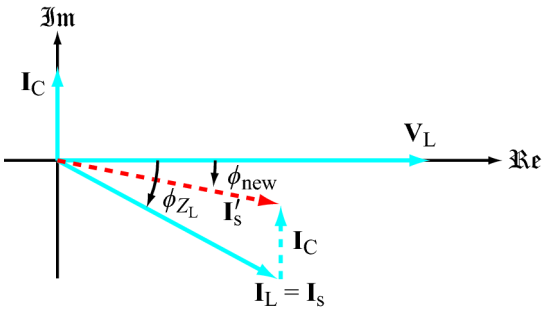


(a) Uncompensated load

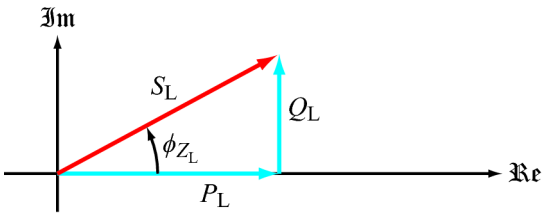


(b) Compensated load

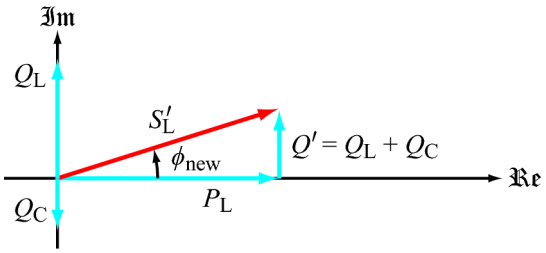
Figure 8.9 Adding a shunt capacitor across an inductive load reduces the current supplied by the generator.



(a) Phasor currents



(b) Uncompensated load



(c) Compensated load

Figure 8.10 Comparison of source currents and ***power factor triangles*** for the compensated and uncompensated circuits.

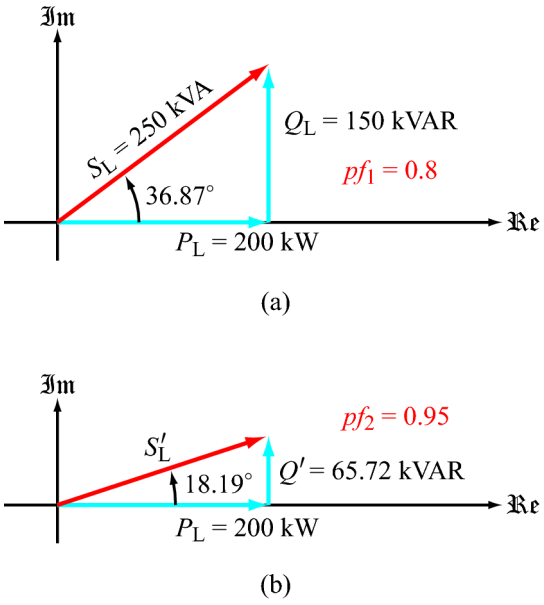


Figure 8.11 Power triangles for Example 8-6.

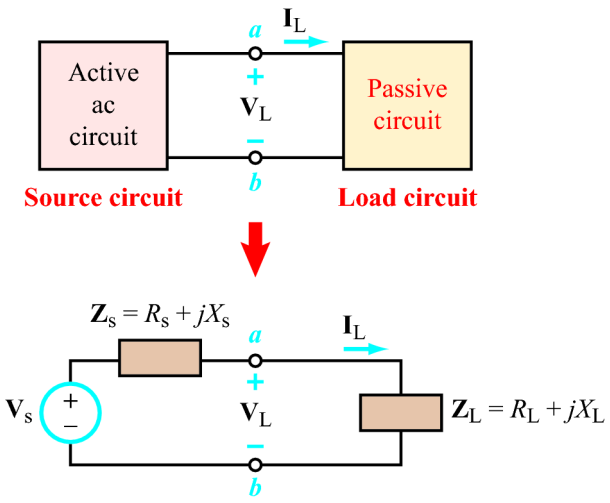


Figure 8.12 Replacing the source and load circuits with their respective Thévenin equivalents.

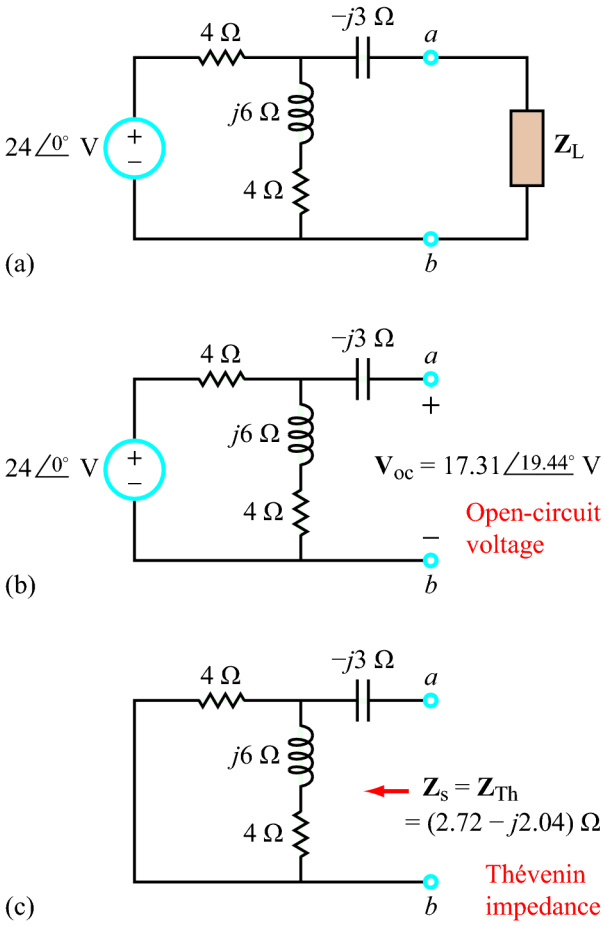


Figure 8.13 Circuit for Example 8-7.

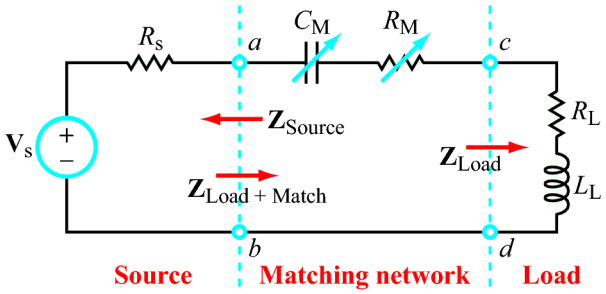


Figure 8.14 Matching network in between the source and the load.

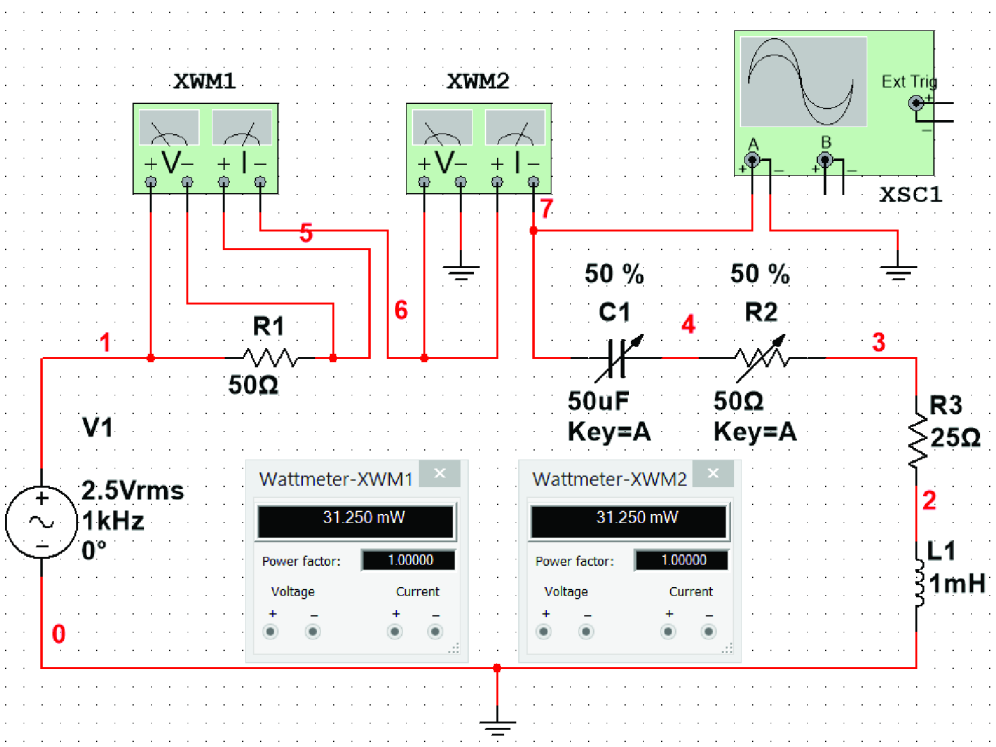


Figure 8.15 Multisim simulation of matching network (CM, RM) in between the source and the load, and wattmeter displays for maximum power transfer.

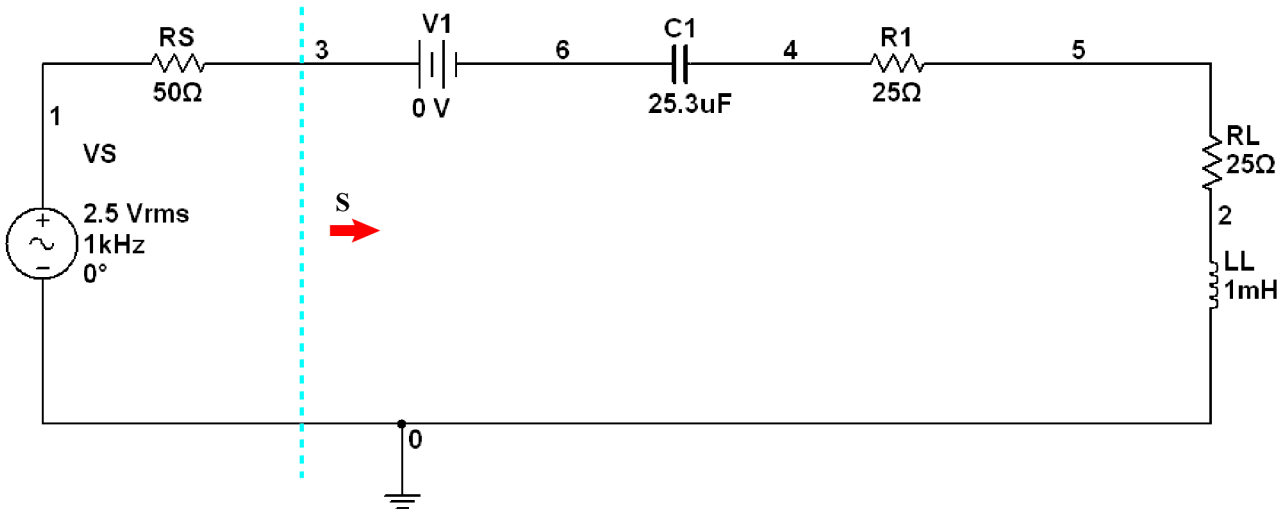


Figure 8.16 Multisim circuit without instruments.

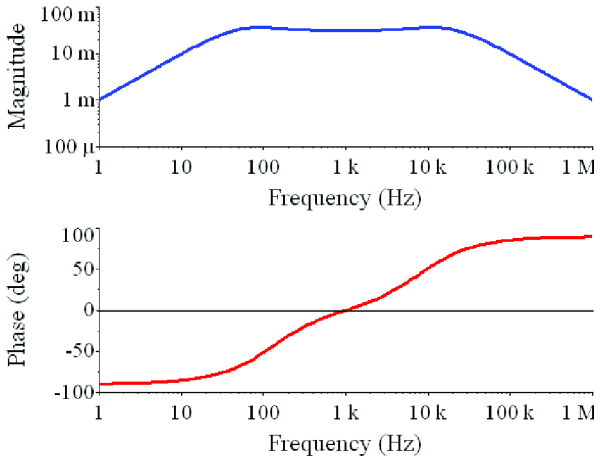


Figure 8.17 Spectral plots of the magnitude and phase of the complex power **S** at terminals (3,0) in **Fig.** 8.16.

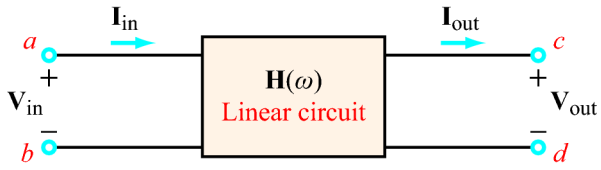
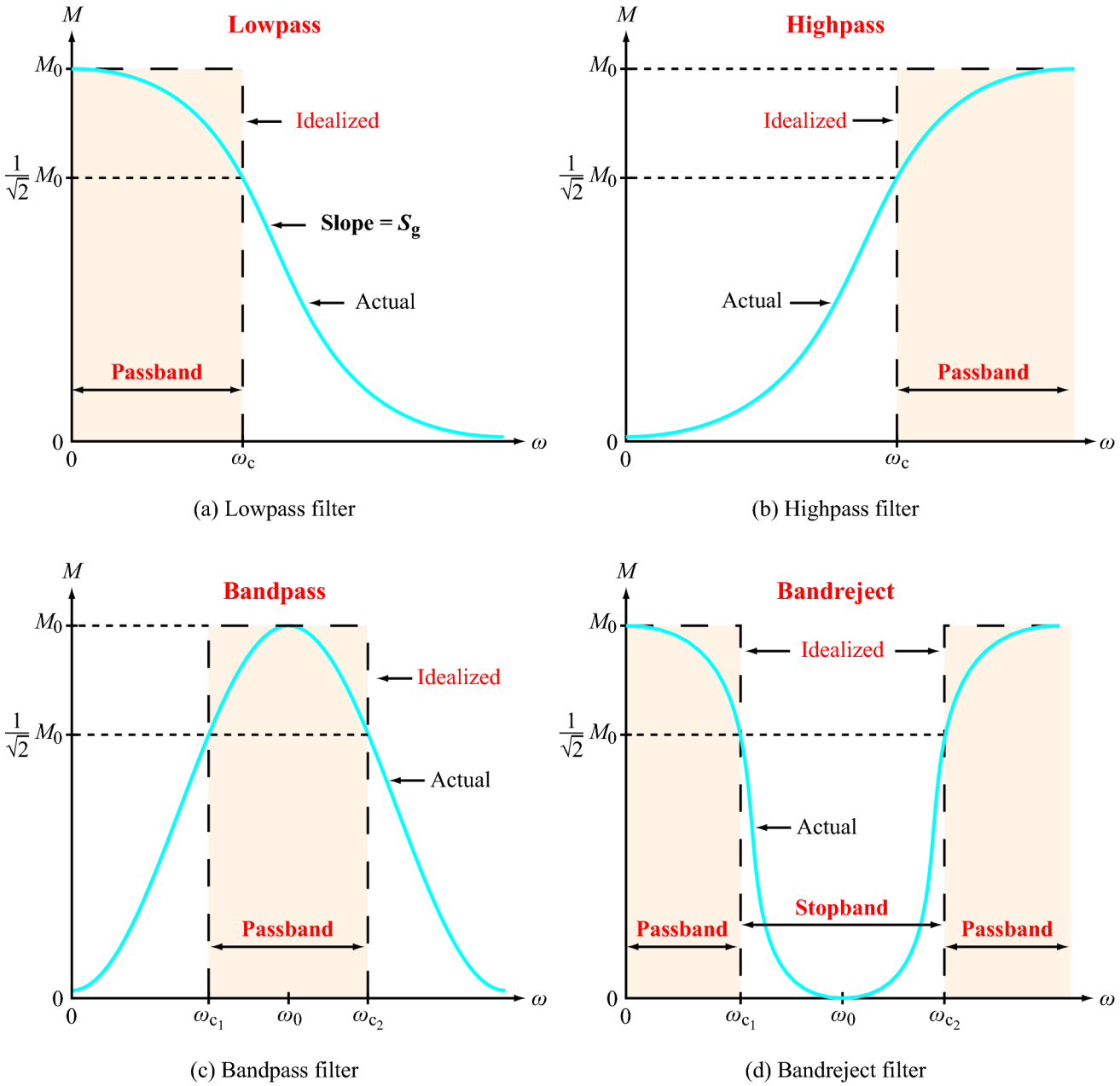


Figure 9.1 The voltage-gain transfer function is $\mathbf{H}(\omega) = \mathbf{V}_{out}(\omega)/\mathbf{V}_{in}(\omega)$.



(a) Lowpass filter

(b) Highpass filter

(c) Bandpass filter

(d) Bandreject filter

Figure 9.2 Typical magnitude spectral responses for the four types of filters.

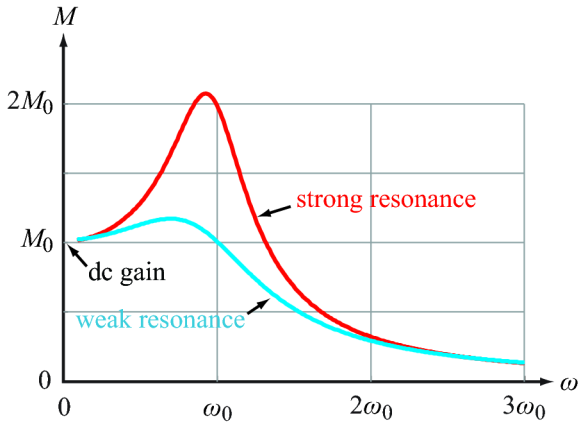
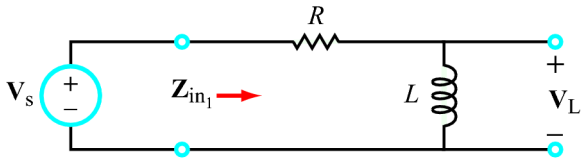
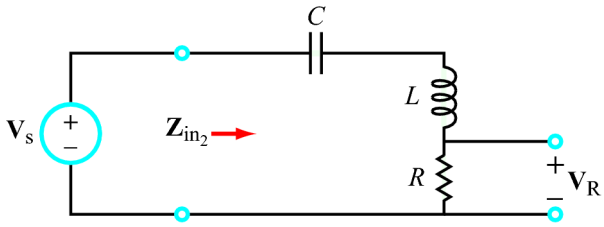


Figure 9.3 Resonant peak in the spectral response of a lowpass filter circuit.

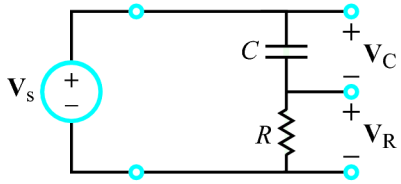


(a) First-order RL filter

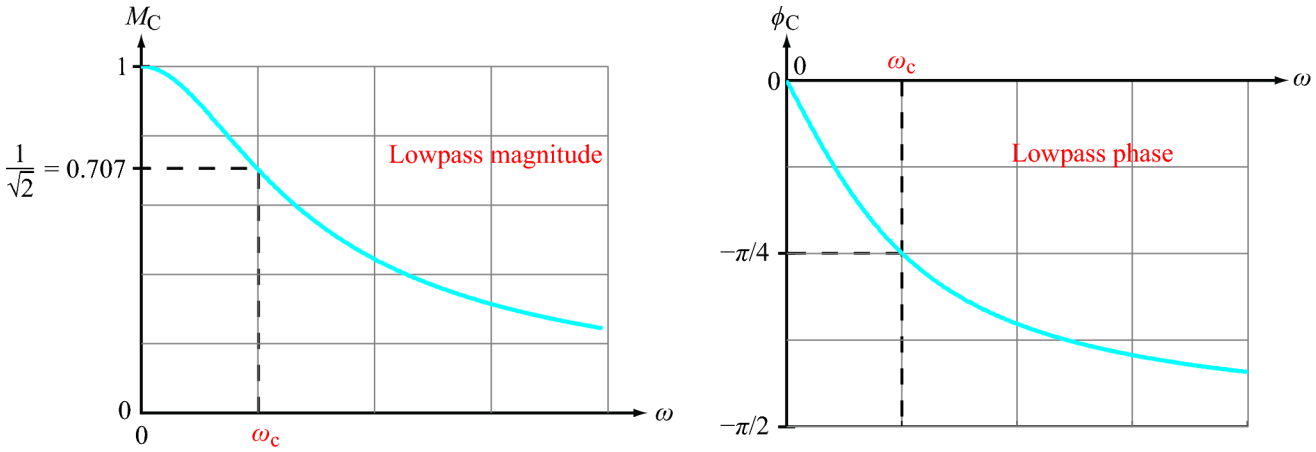


(b) Series RLC circuit

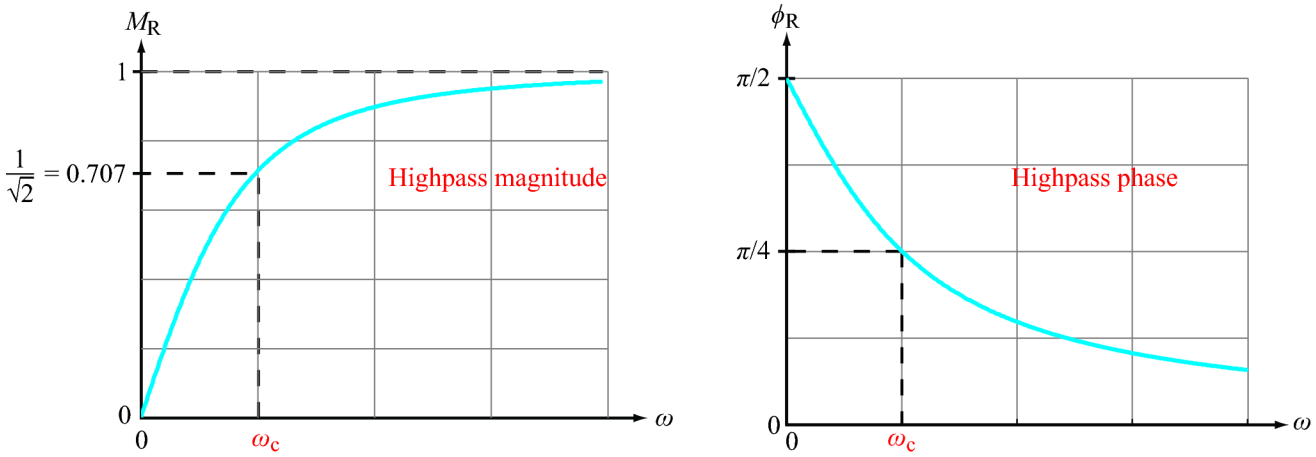
Figure 9.4 Resonance occurs when the imaginary part of the input impedance is zero. For the RL circuit, $\mathfrak{Im}[\mathbf{Z}_{in_1}] = 0$ when $\omega = 0$ (dc), but for the RLC circuit, $\mathfrak{Im}[\mathbf{Z}_{in_2}] = 0$ requires that $\mathbf{Z}_L = -\mathbf{Z}_C$ or, equivalently, $\omega^2 = 1/LC$.



(a) RC circuit



(b) Magnitude and phase angle of $\mathbf{H}_C(\omega) = \mathbf{V}_C / \mathbf{V}_s$



(c) Magnitude and phase angle of $\mathbf{H}_R(\omega) = \mathbf{V}_R / \mathbf{V}_s$

Figure 9.5 Lowpass and highpass transfer functions.

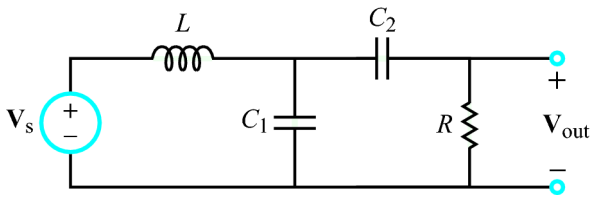


Figure 9.6 Circuit of Example 9-1.

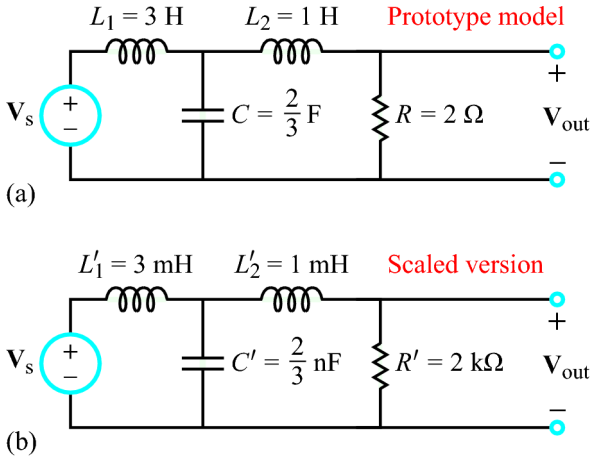


Figure 9.7 Prototype and scaled circuits of Example 9-2.

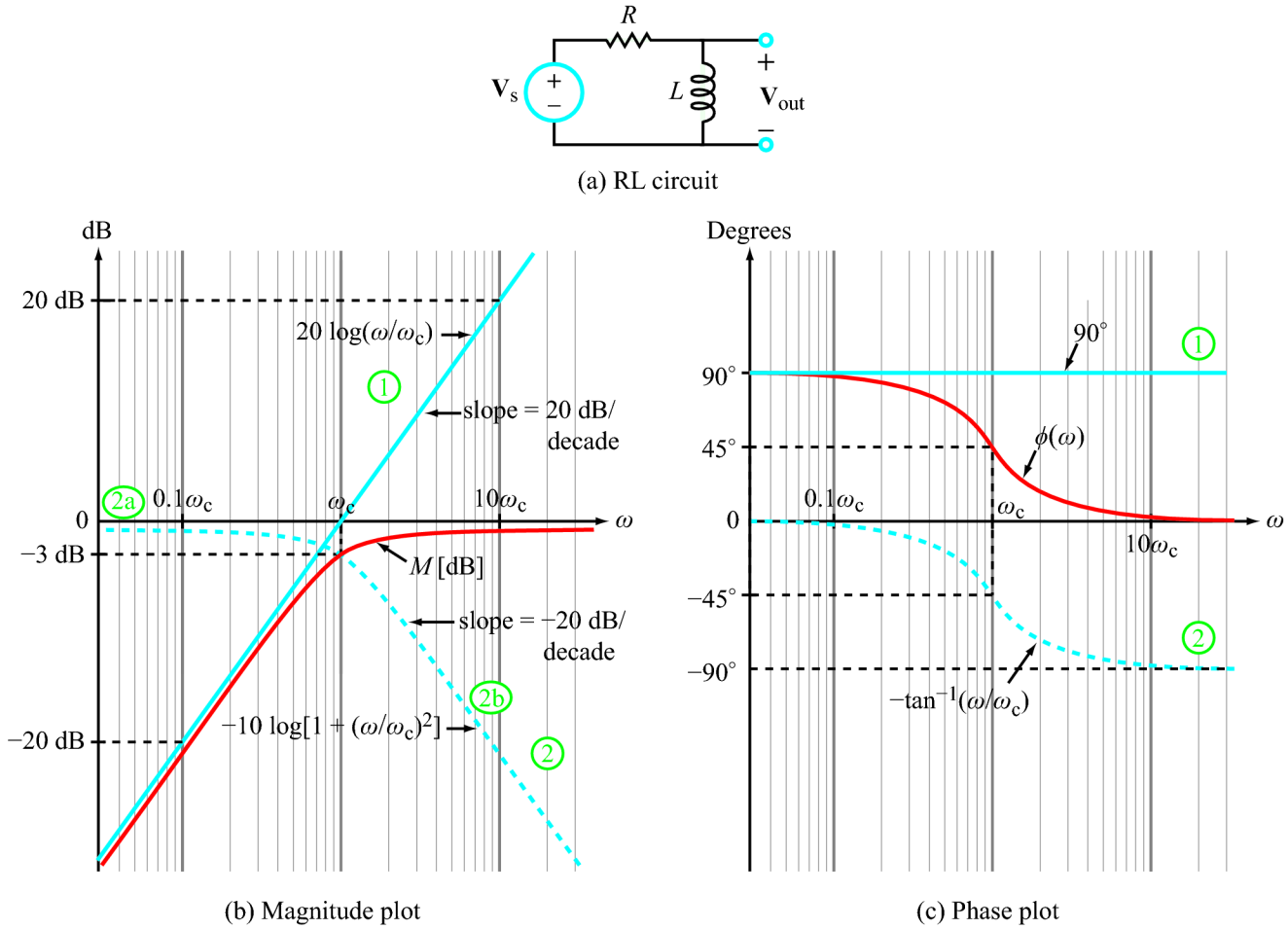


Figure 9.8 Magnitude and phase plots of $\mathbf{H} = \mathbf{V}_{out}/\mathbf{V}_s$.

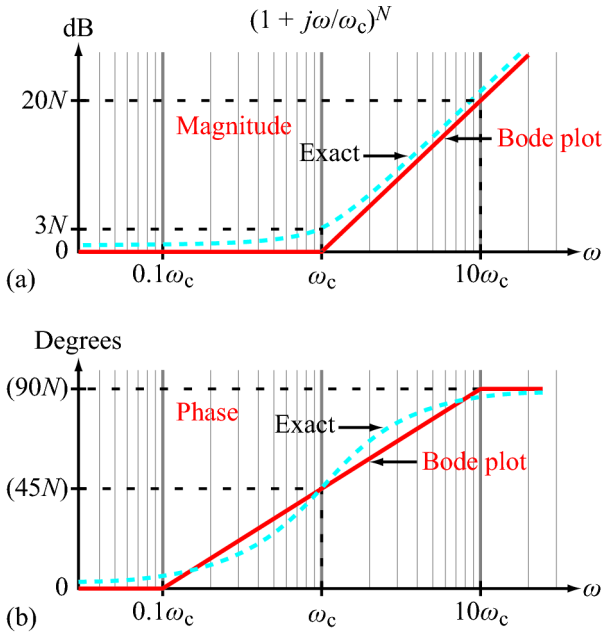


Figure 9.9 Comparison of exact plots with the Bode straight-line approximations for a simple zero with a corner frequency ω_c.

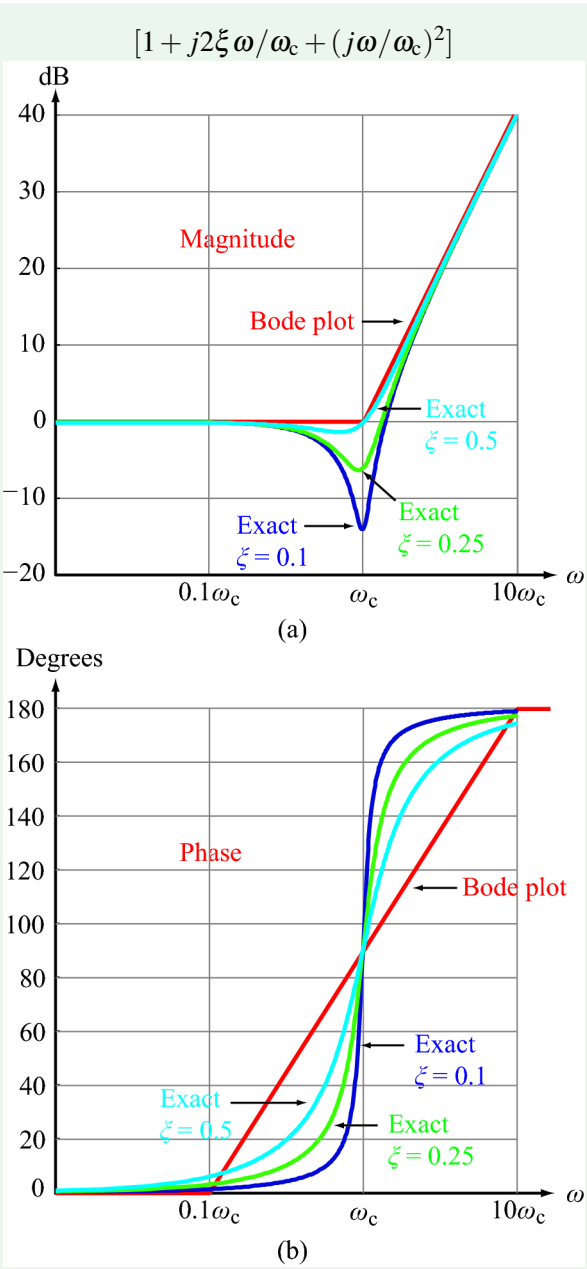


Figure 9.10 Comparison of exact plots with Bode straight-line approximations for a quadratic zero $[1 + j2\xi\omega/\omega_c + (j\omega/\omega_c)^2]$.

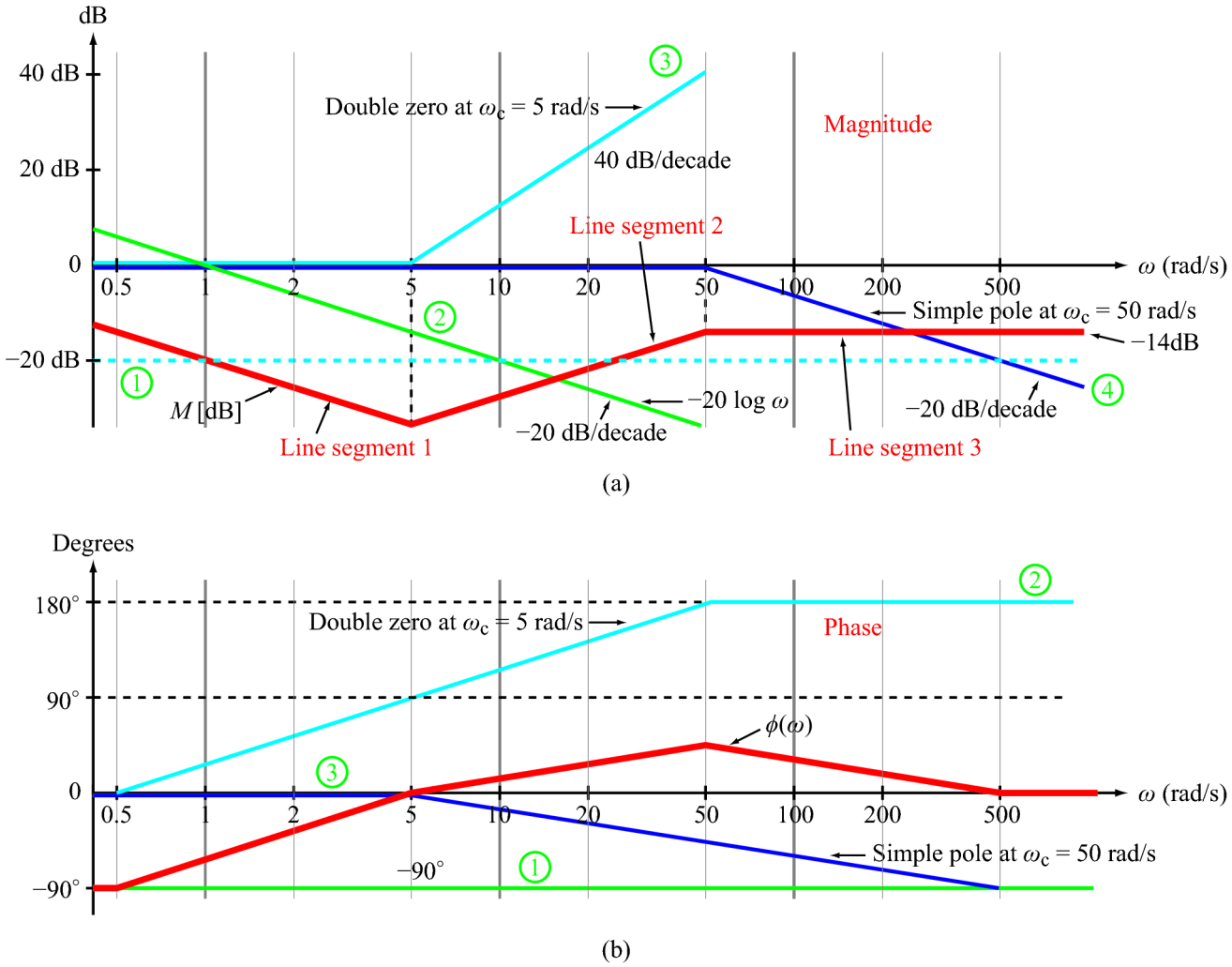


Figure 9.11 Bode amplitude and phase plots for the transfer function of Example 9-4.

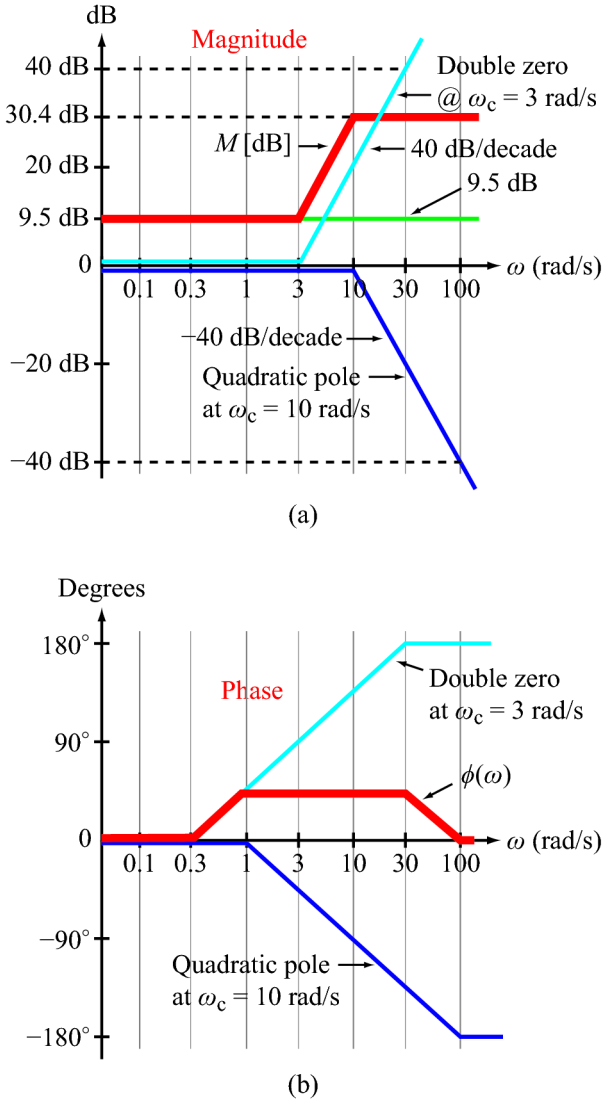


Figure 9.12 Bode magnitude and phase plots for Example 9-5.

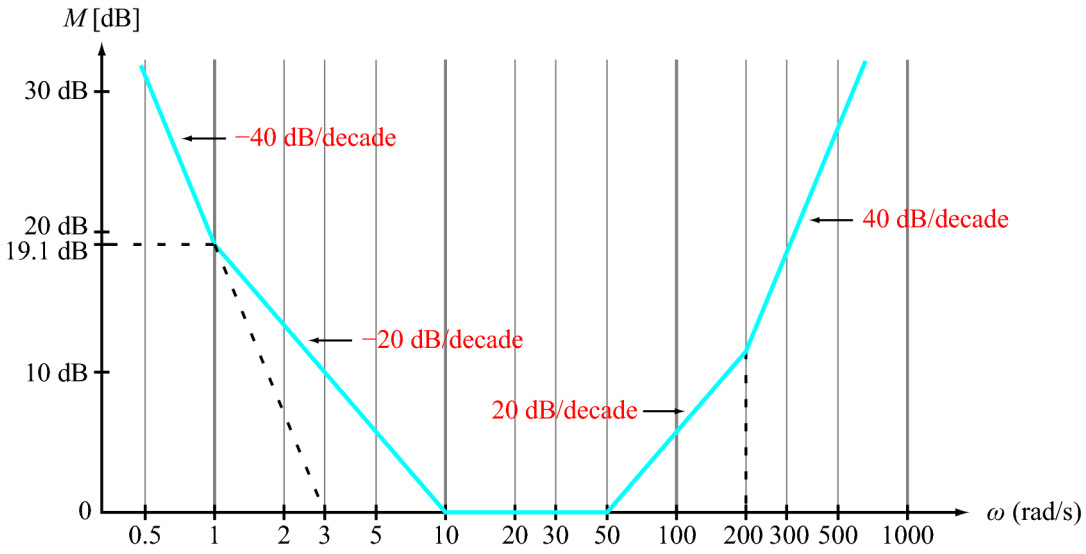


Figure 9.13 Bode plot of bandreject filter of Example 9-6.

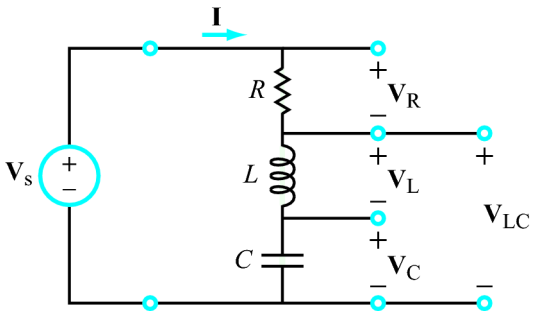
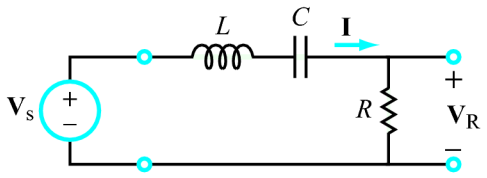
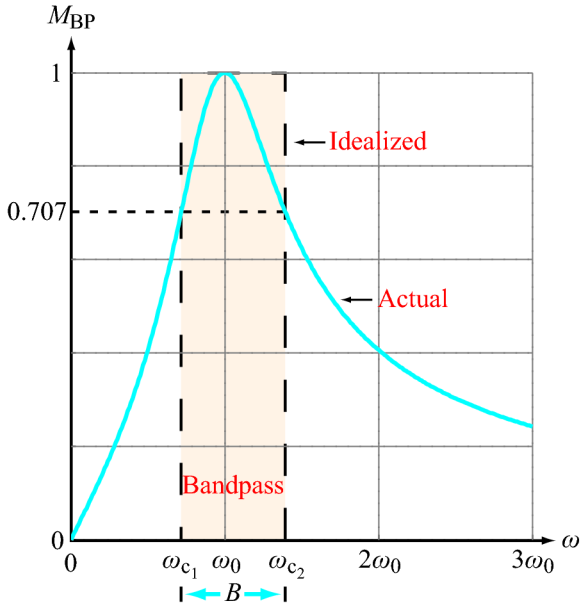


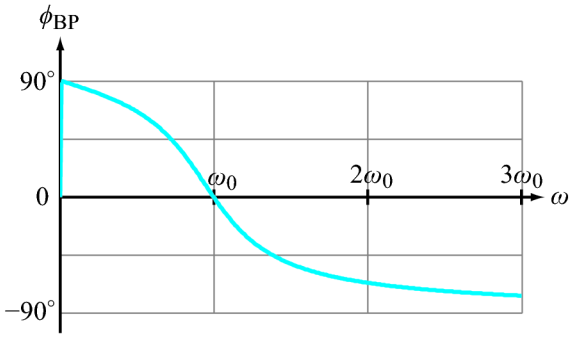
Figure 9.14 Series RLC circuit.



(a) RLC circuit



(b) $M_{BP}(\omega)$



(c) $\phi_{BP}(\omega)$

Figure 9.15 Series RLC bandpass filter.

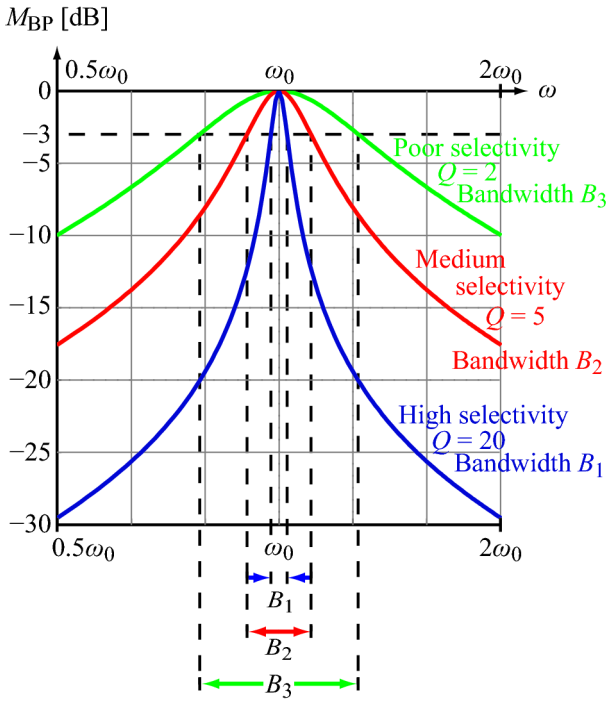


Figure 9.16 Examples of bandpass-filter responses.

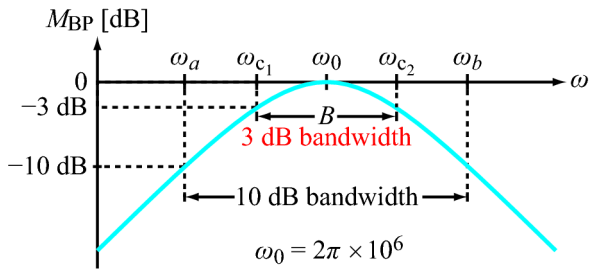
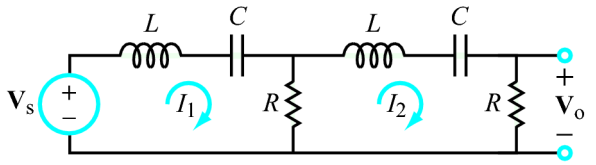
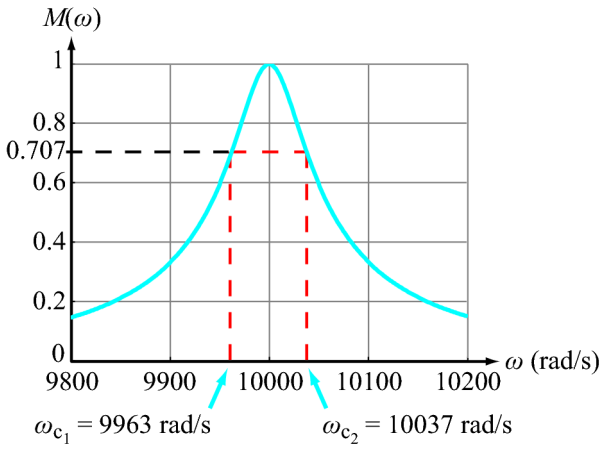


Figure 9.17 10 dB bandwidth extends from ω_a to ω_b, corresponding to $M_{\text{BP}}\,(\text{dB}) = -10$ dB.

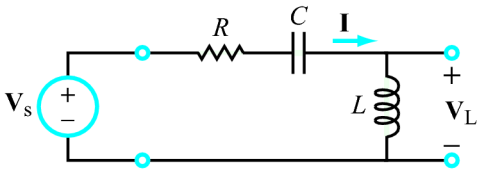


(a) Two-stage circuit

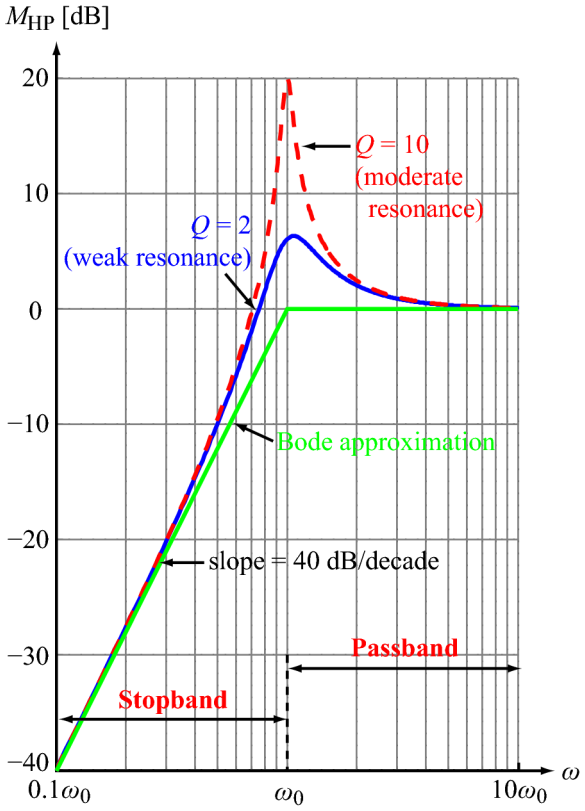


(b) $M(\omega)$

Figure 9.18 Two-stage RLC circuit of Example 9-8.

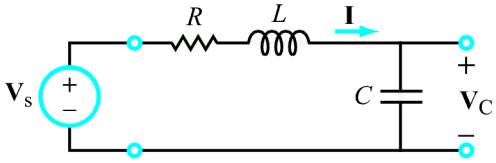


(a) $\mathbf{H}_{HP} = \mathbf{V}_L / \mathbf{V}_s$

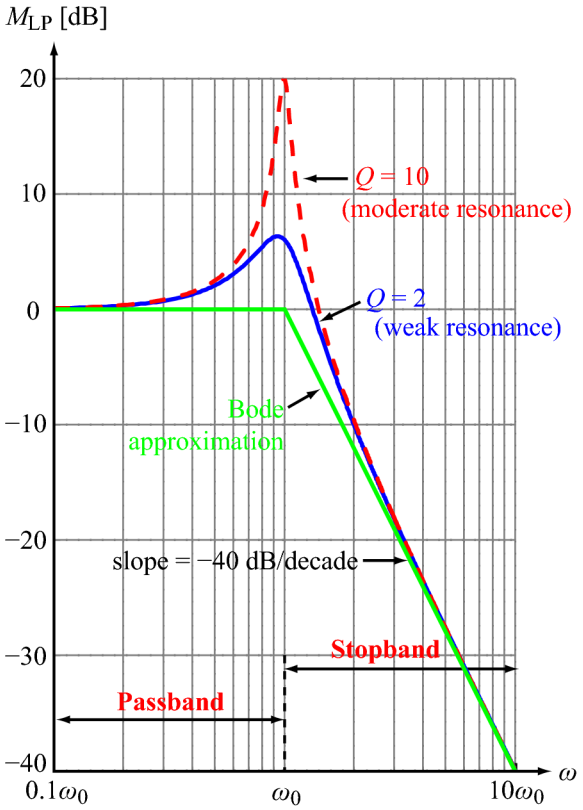


(b) Magnitude spectrum

Figure 9.19 Plots of M_{HP} [dB] for $Q = 2$ (weak resonance) and $Q = 10$ (moderate resonance).

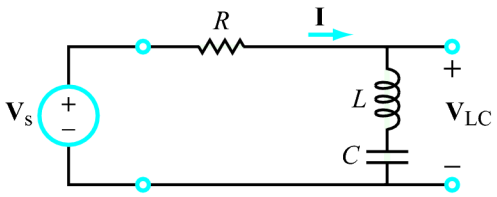


(a) $\mathbf{H}_{LP} = \mathbf{V}_C / \mathbf{V}_s$

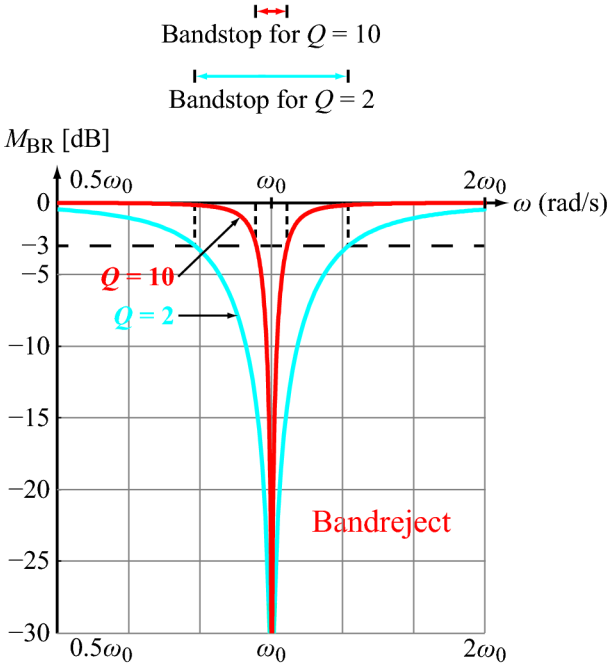


(b) Magnitude spectrum

Figure 9.20 RLC lowpass filter.



(a) $\mathbf{H}_{BR} = \mathbf{V}_{LC}/\mathbf{V}_s$



(b) Spectral response

Figure 9.21 Bandreject filter.

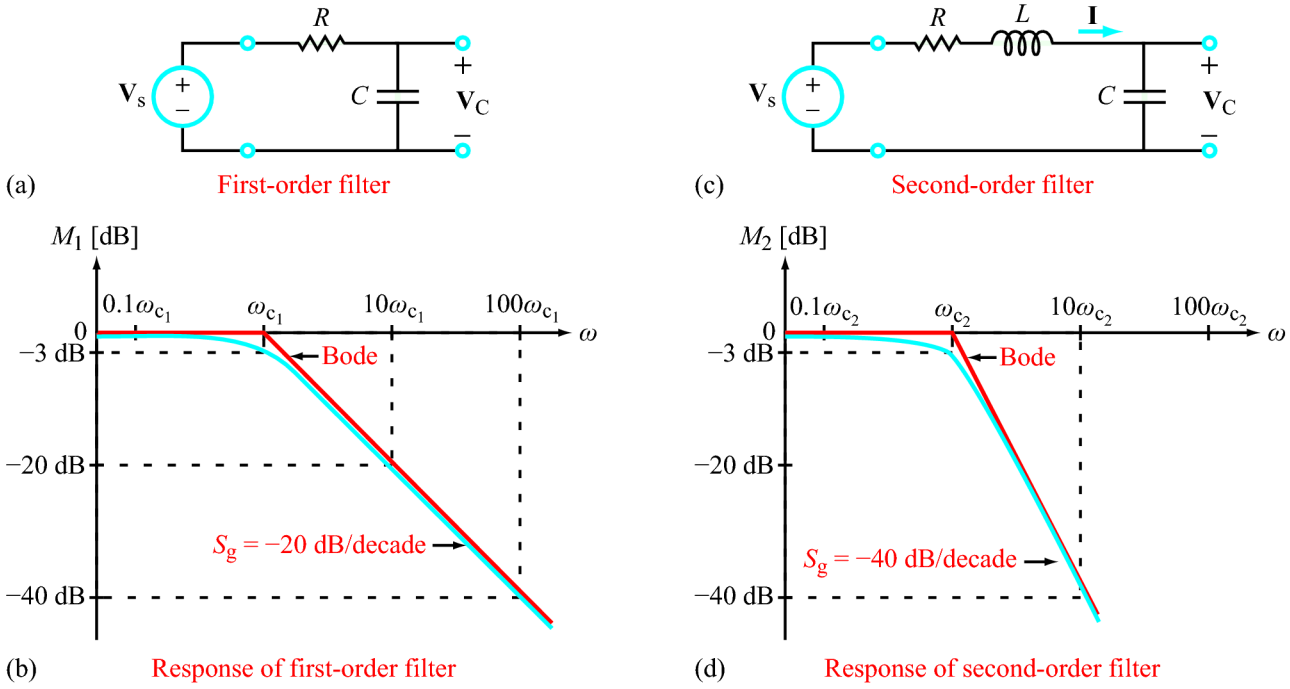
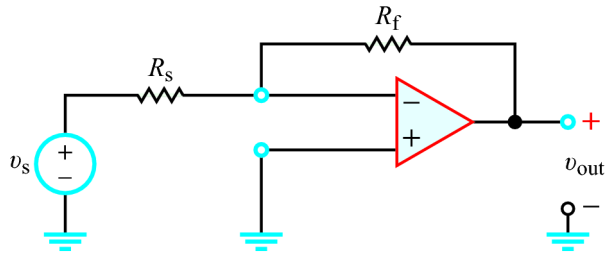
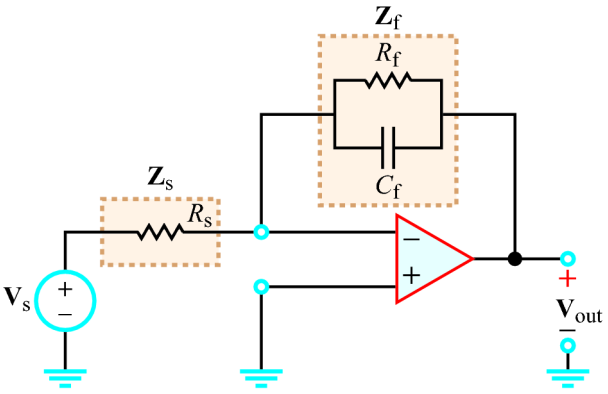


Figure 9.22 Comparison of magnitude responses of the first-order RC filter and the second-order RLC filter. The corner frequencies are given by $\omega_{c_1} = 1/RC$ and $\omega_{c_2} = 1.28/RC$.



(a) Inverting amplifier



(b) Phasor domain with impedances

Figure 9.23 Inverting amplifier functioning like a lowpass filter.

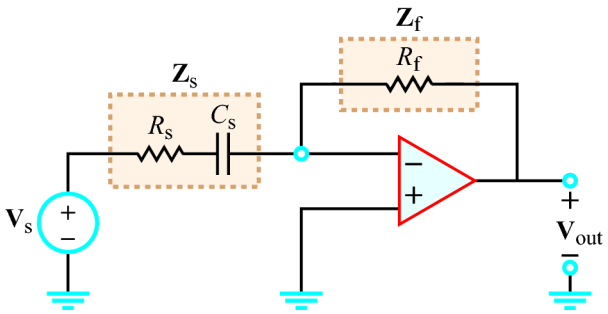
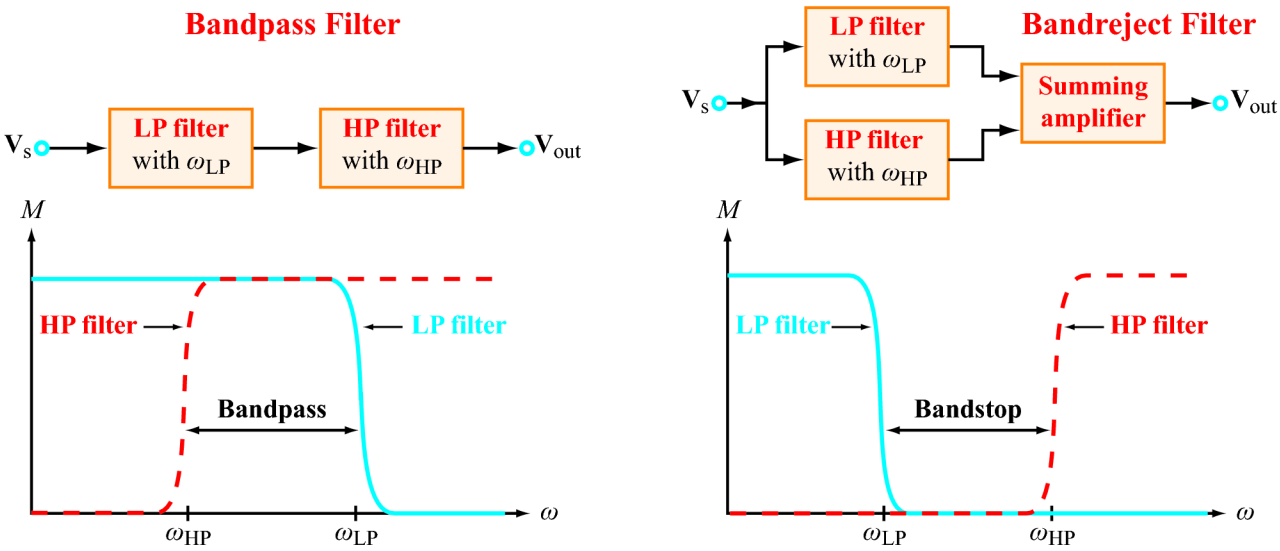


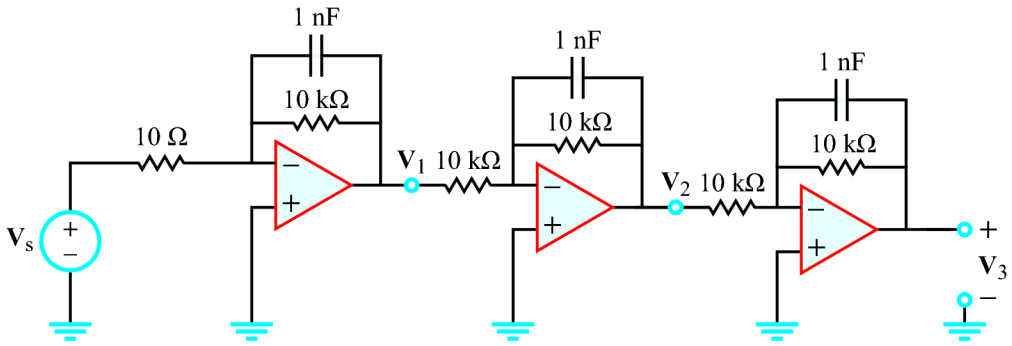
Figure 9.24 Single-pole active highpass filter.



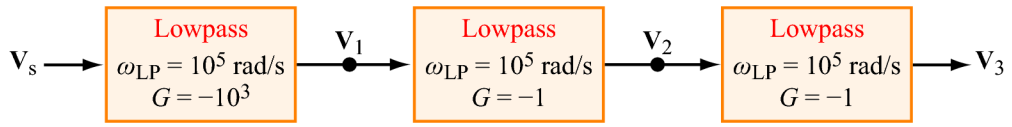
(a) Bandpass filter (note that $\omega_{LP} > \omega_{HP}$)

(b) Bandreject filter

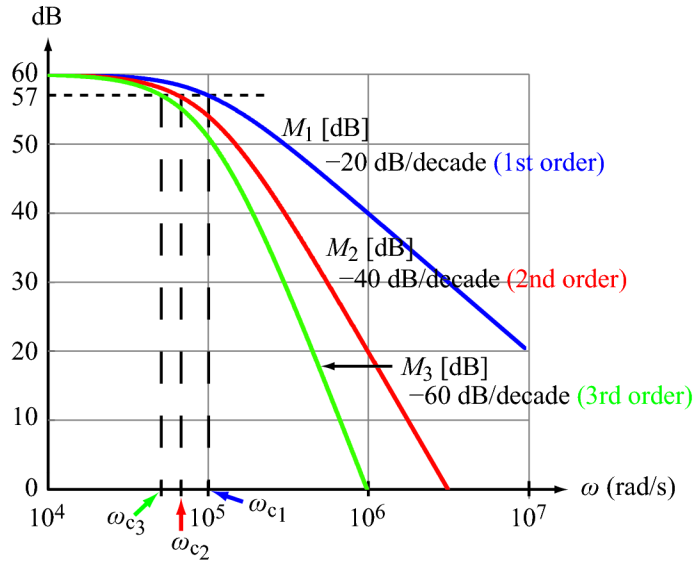
Figure 9.25 (a) In-series cascade of a lowpass and a highpass filter generates a bandpass filter; (b) in-parallel cascading generates a bandreject filter.



(a) Circuit diagram

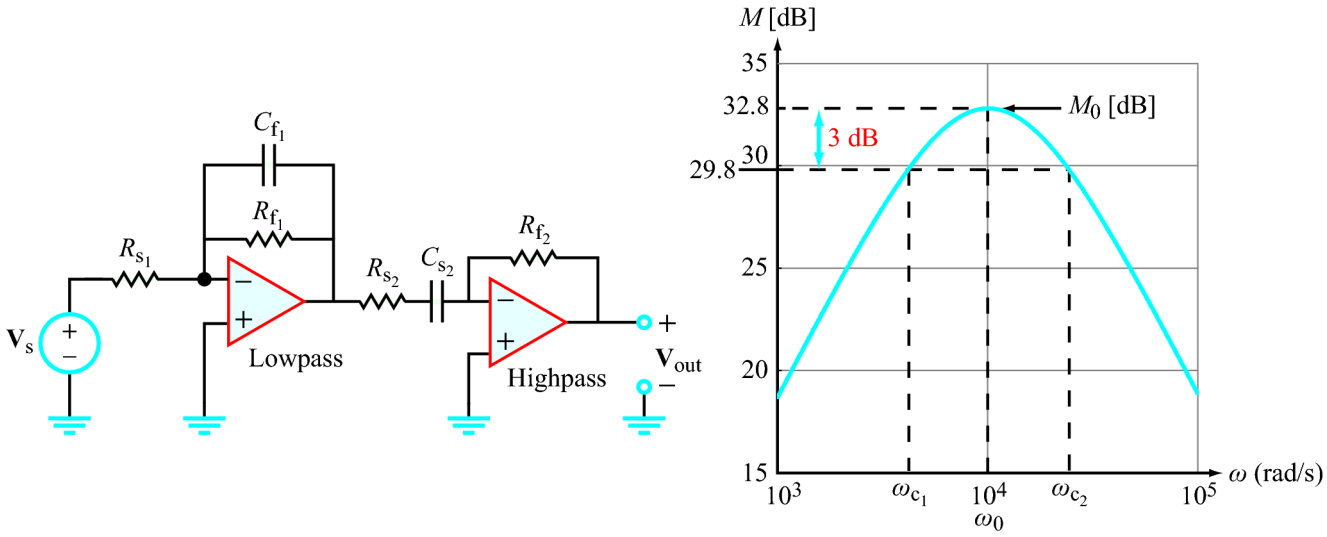


(b) Block diagram



(c) Transfer function plots

Figure 9.26 Three-stage lowpass filter and corresponding transfer functions.



(a) Two-stage bandpass filter

(b) M [dB]

Figure 9.27 Active bandpass filter of Example 9-11.

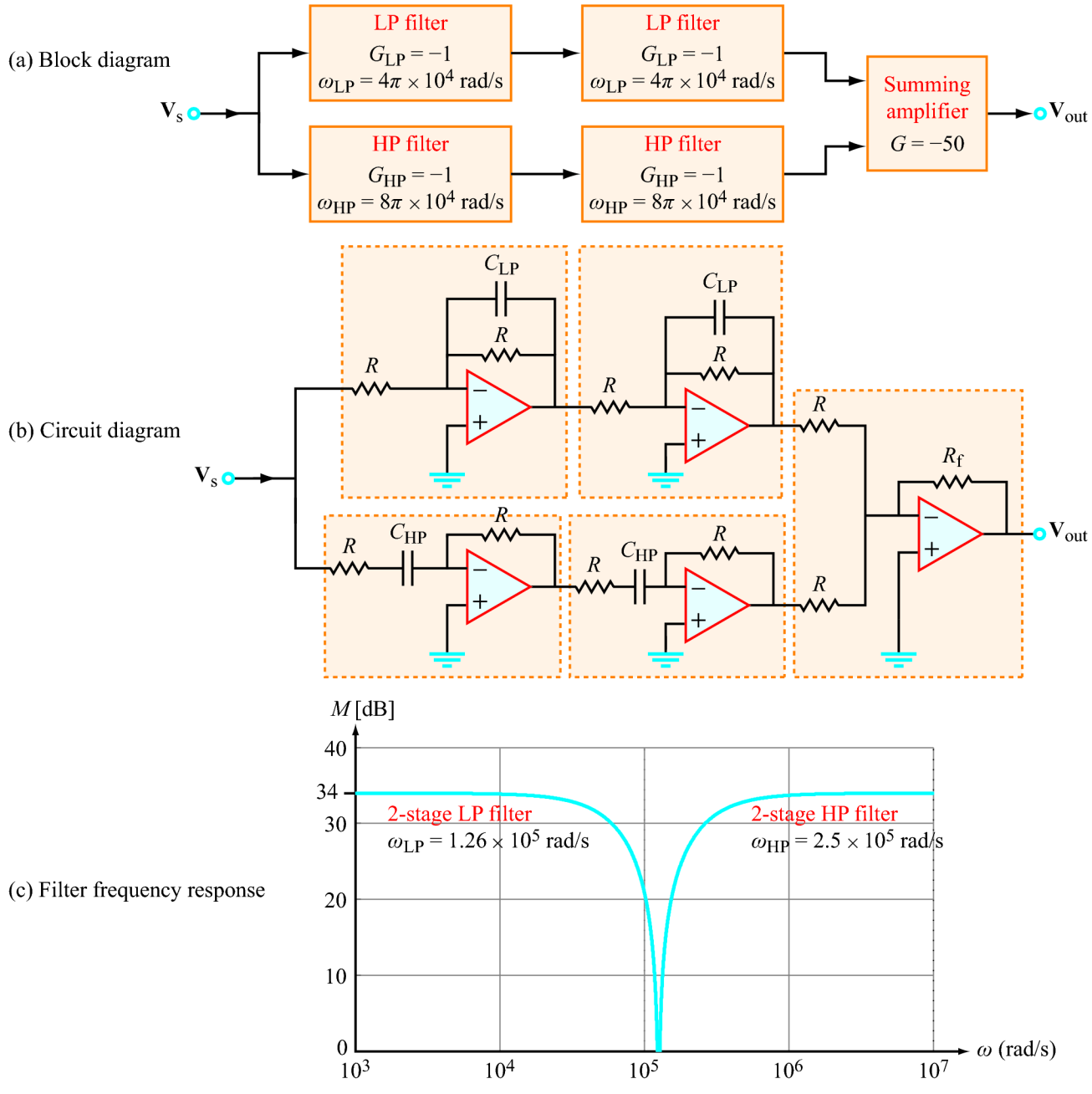
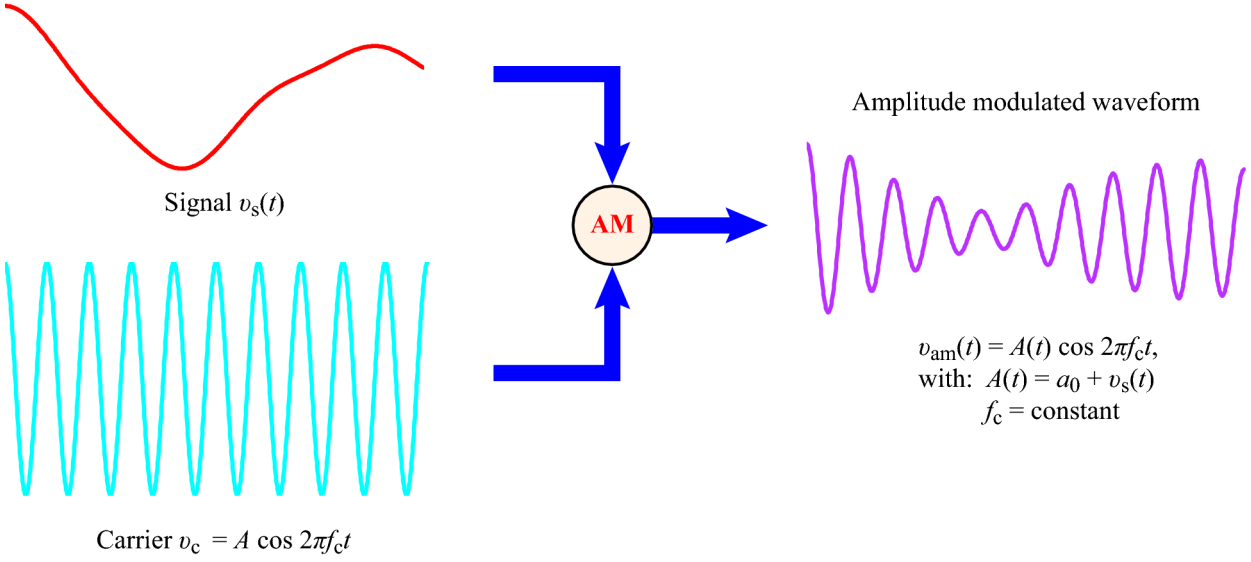
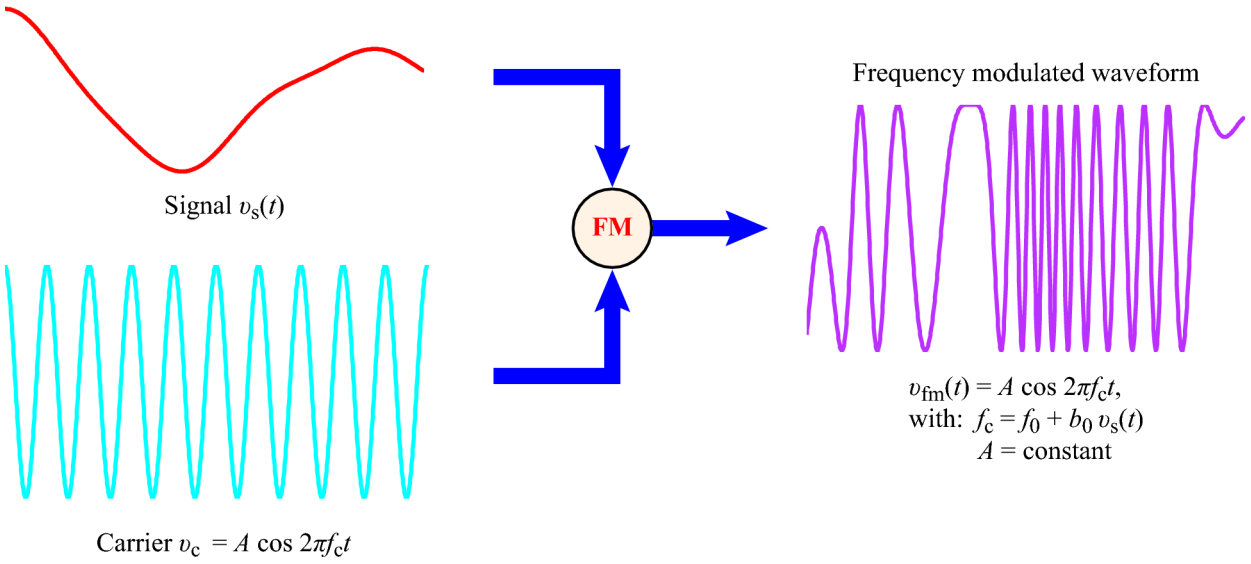


Figure 9.28 Bandreject filter of Example 9-12.



(a) AM



(b) FM

Figure 9.29 Overview of AM and FM.

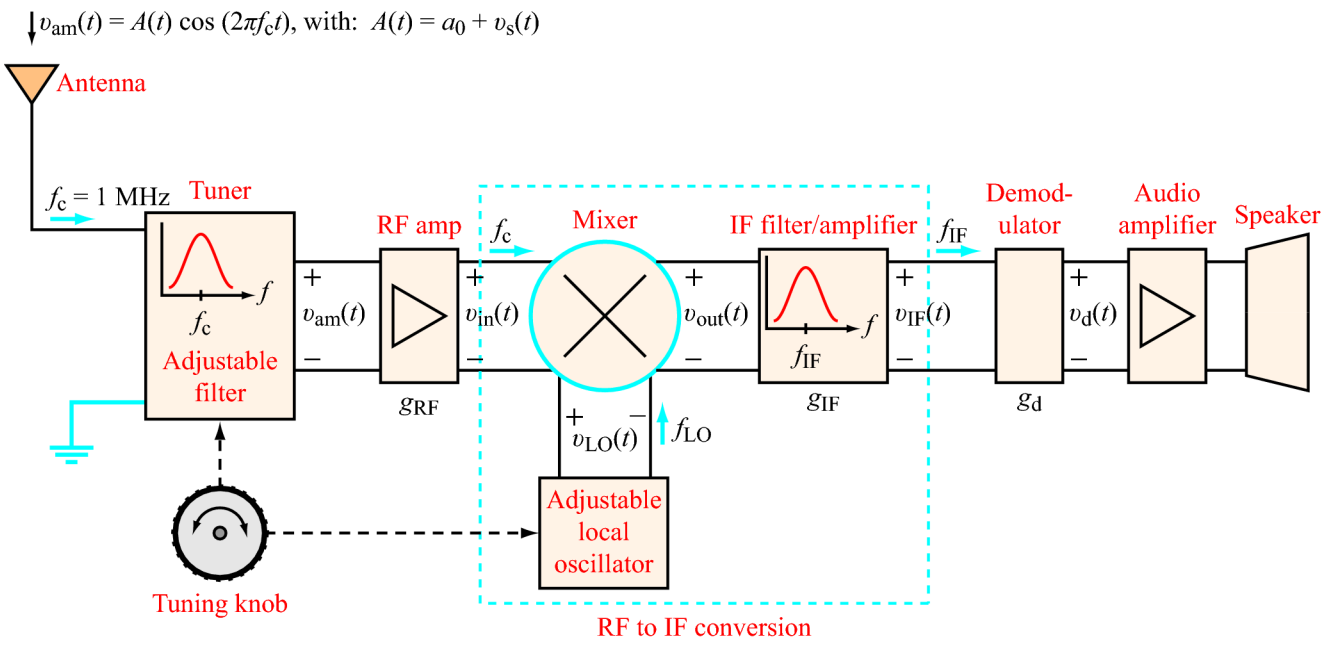


Figure 9.30 Block diagram of superheterodyne receiver.

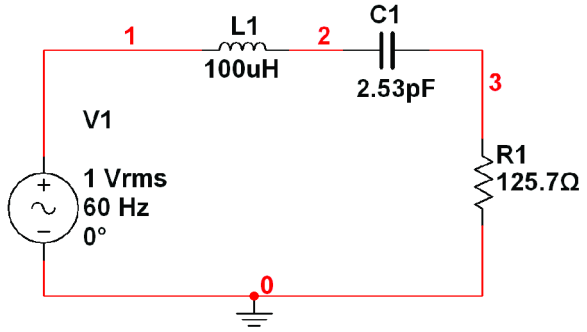


Figure 9.31 A series RLC filter implemented in Multisim.

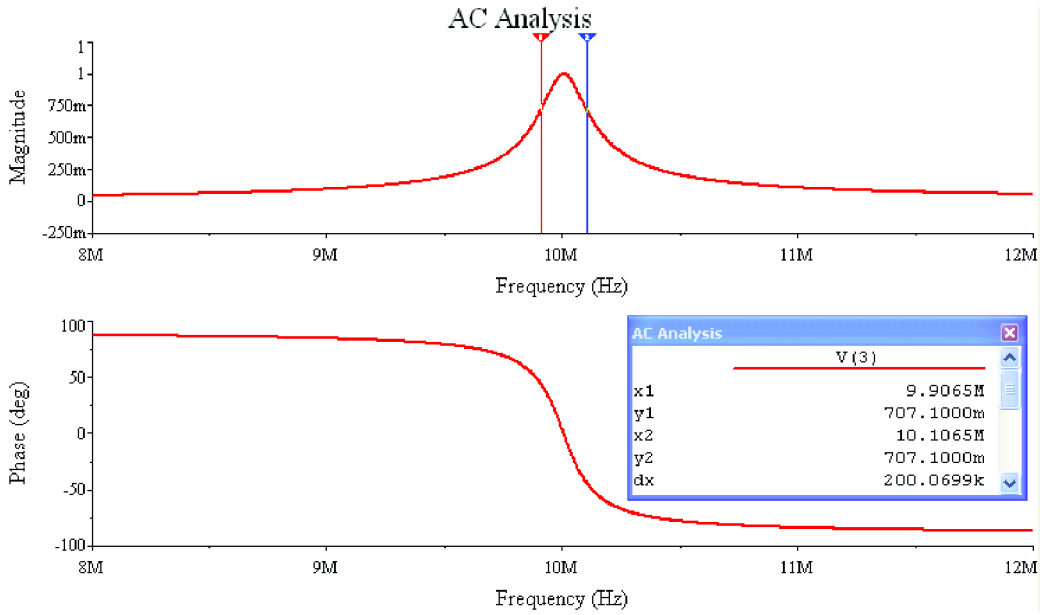


Figure 9.32 Magnitude and phase plots for the circuit of **Fig.** 9.31 generated by AC Analysis for Example 9-13.

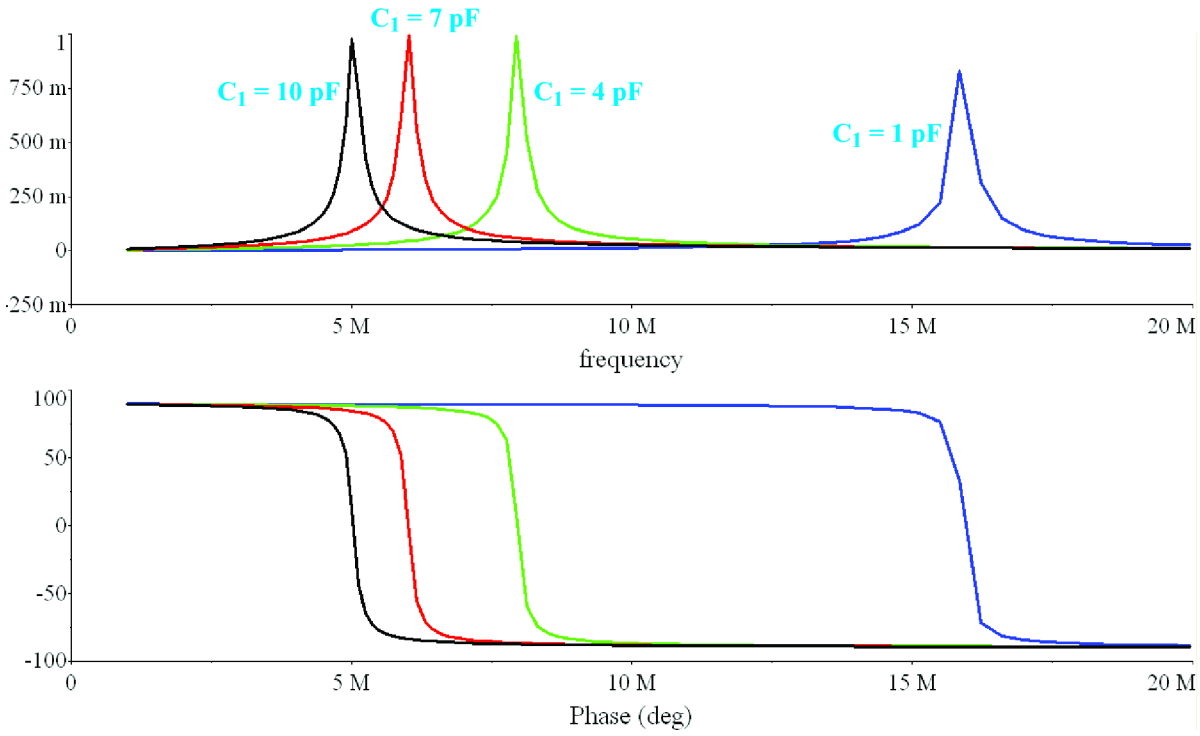
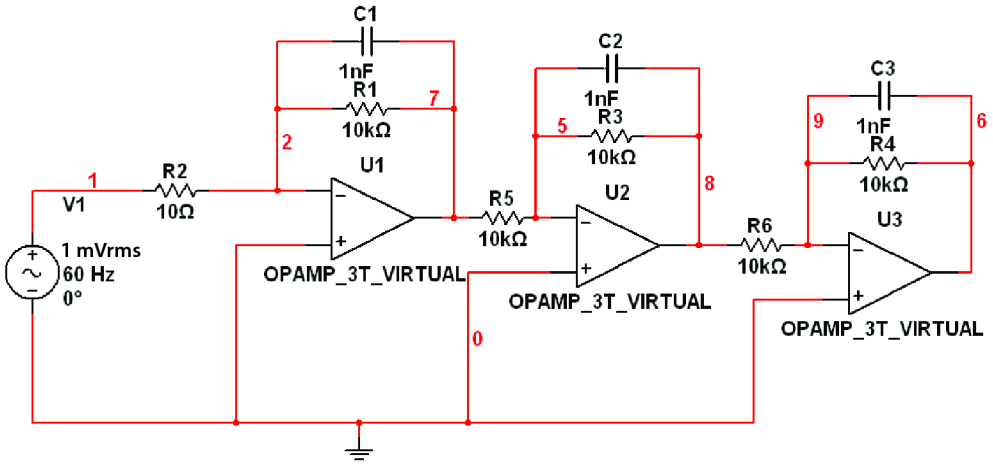
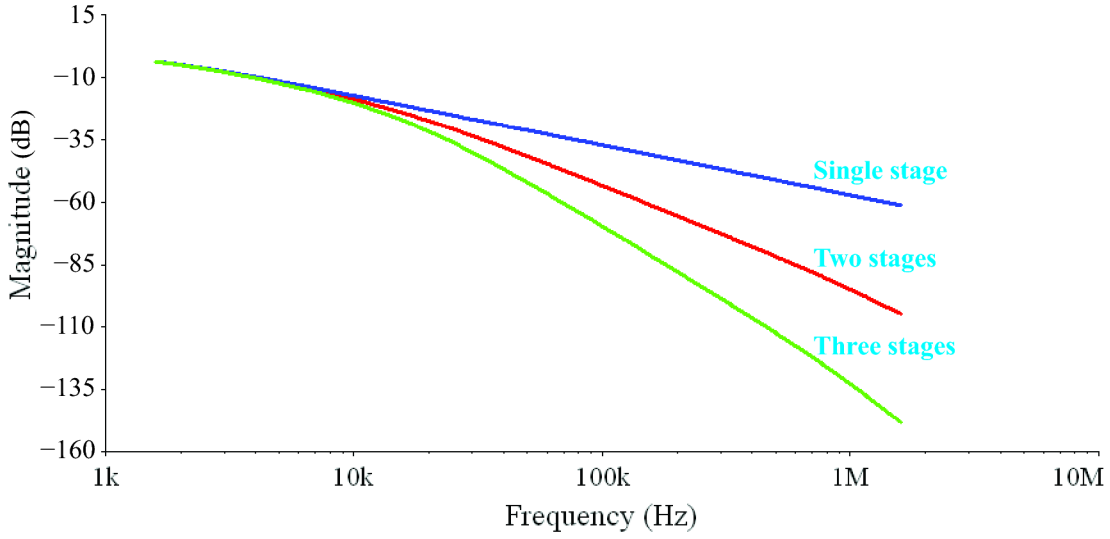


Figure 9.33 AC analysis plots for the circuit in **Fig.** 9.31 generated with the Parameter Sweep tool in Example 9-14. The capacitance was varied from 1 to 10 pF.

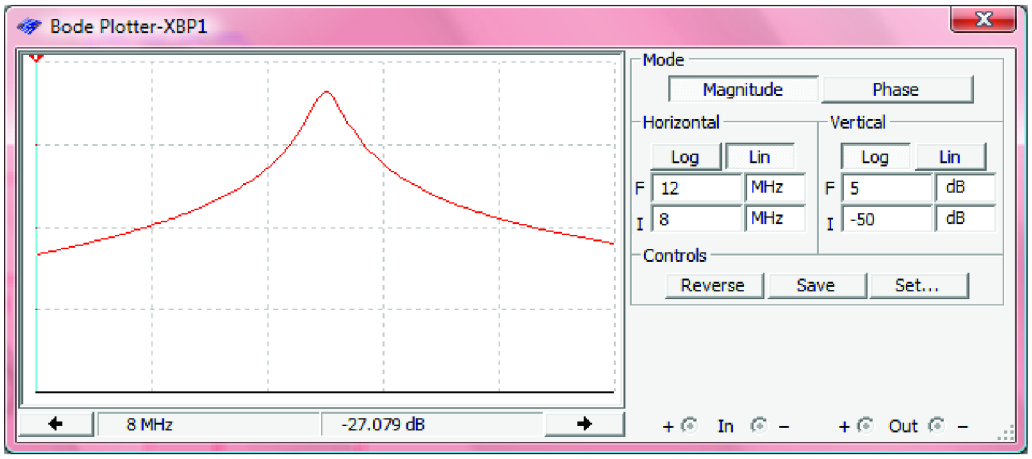


(a) Three-stage circuit of Fig. 9-26(a)



(b) Bode plots

Figure 9.34 Three-stage op-amp circuit of **Fig.** 9.26**(a)** reproduced in Multisim for Example 9-15.



(a) Magnitude plot

(b) Phase plot

Figure 9.35 Output of Bode Plotter Instrument for Example 9-16.

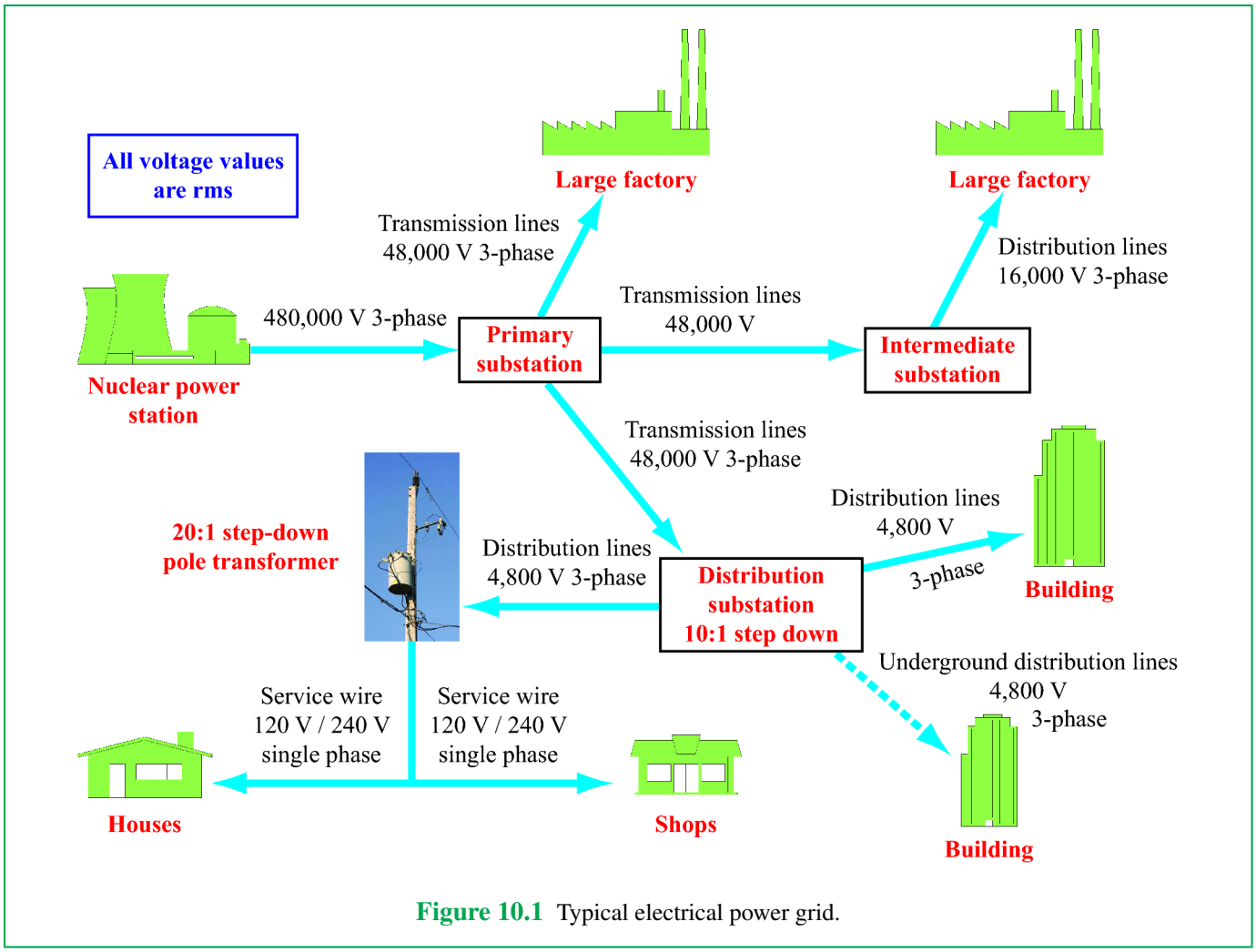


Figure 10.1 Typical electrical power grid.

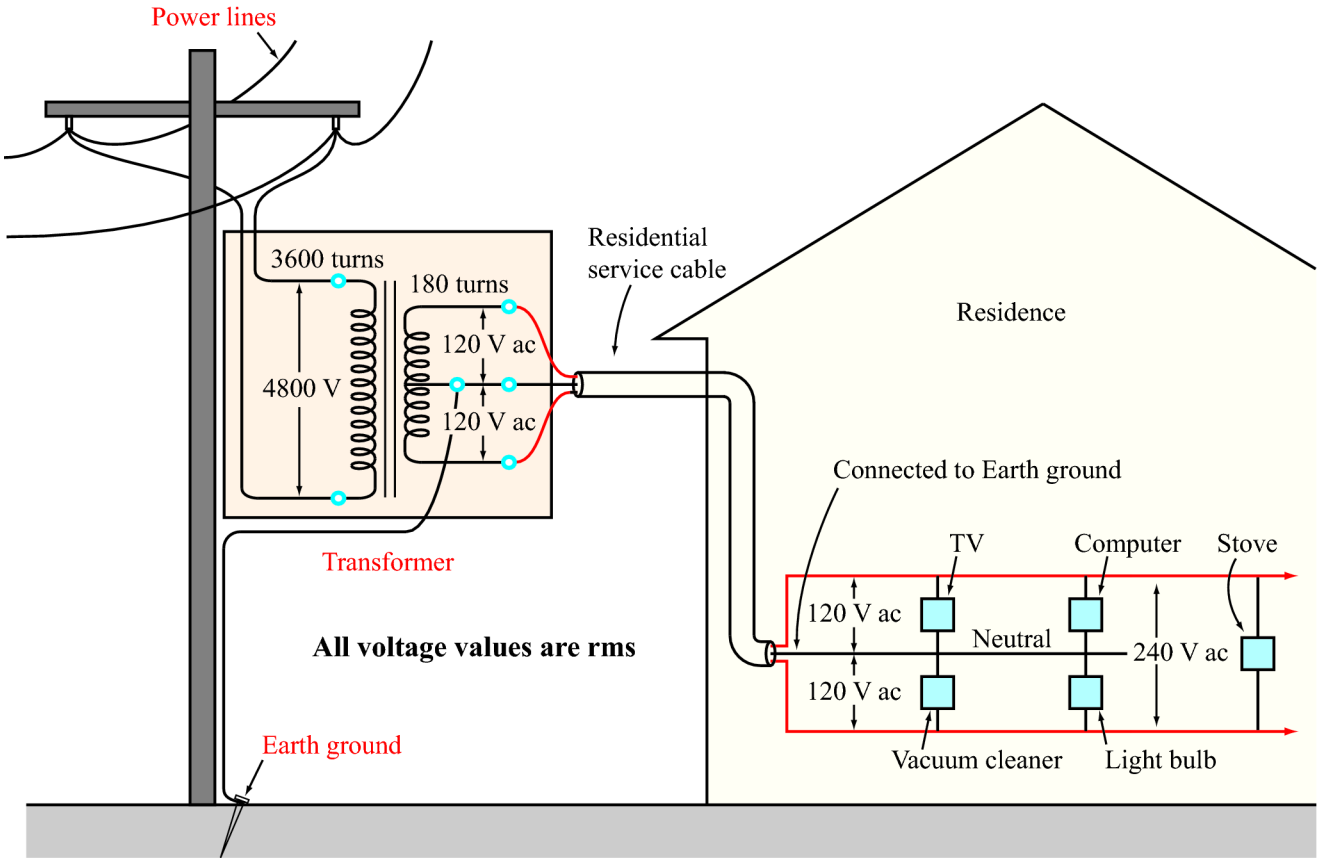
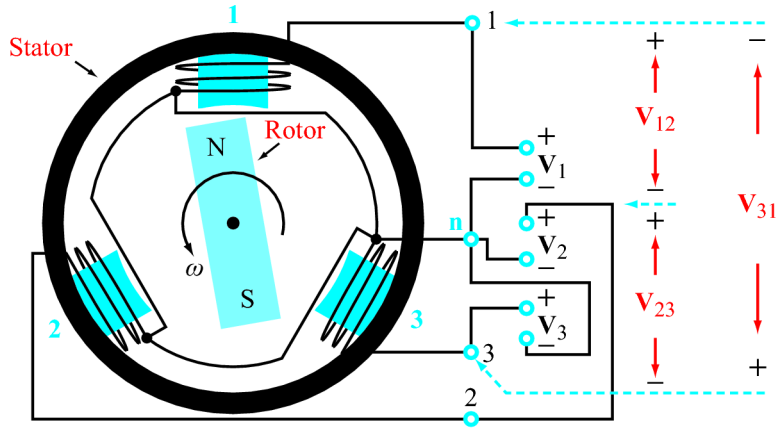
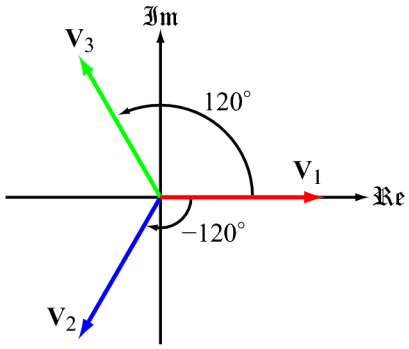


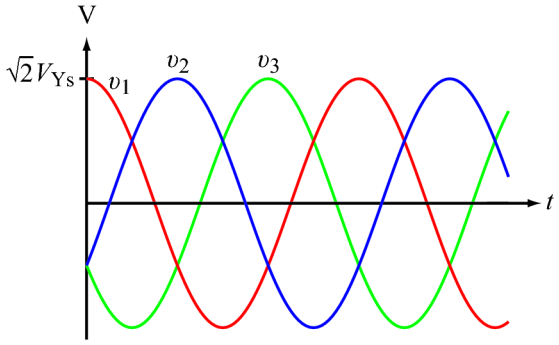
Figure 10.2 A 4800 V rms single-phase ac source connected to a residential user through a 20 : 1 step-down transformer.



(a) Three-phase generator

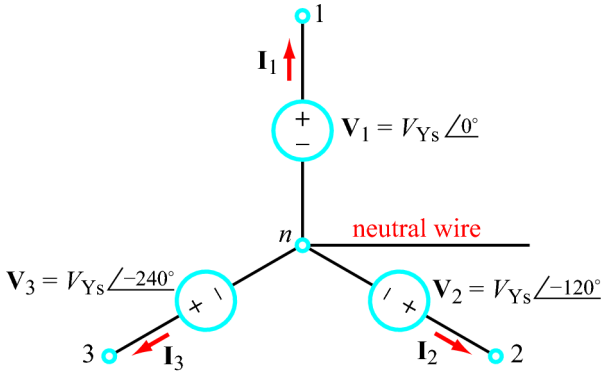


(b) Phasor voltages $\mathbf{V}_1$ to $\mathbf{V}_3$ in the complex plane

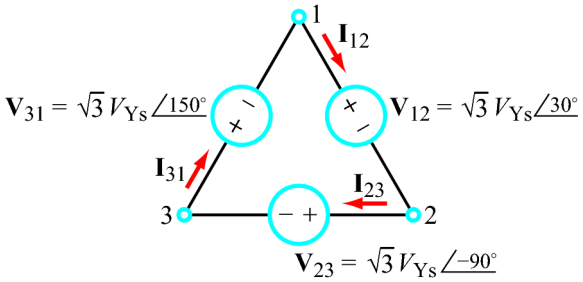


(c) Voltage waveforms

Figure 10.3 Three-phase ac generator and associated voltage waveforms.

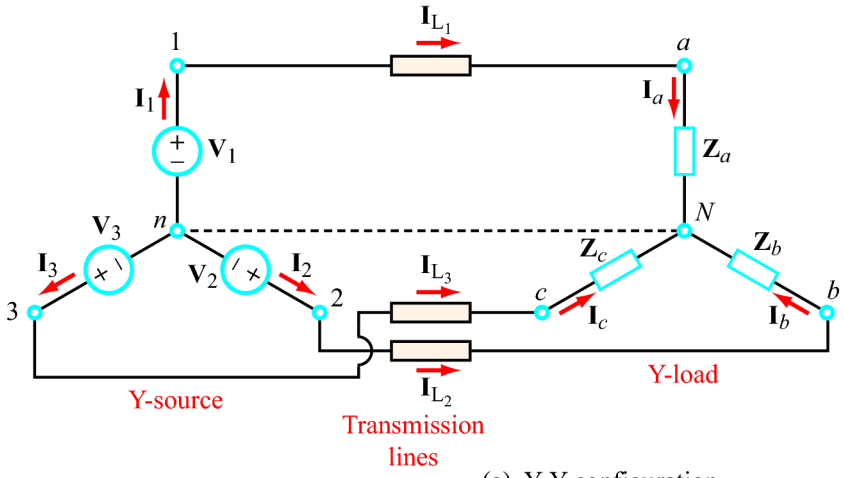


(a) Y-source configuration



(b) Δ-source configuration

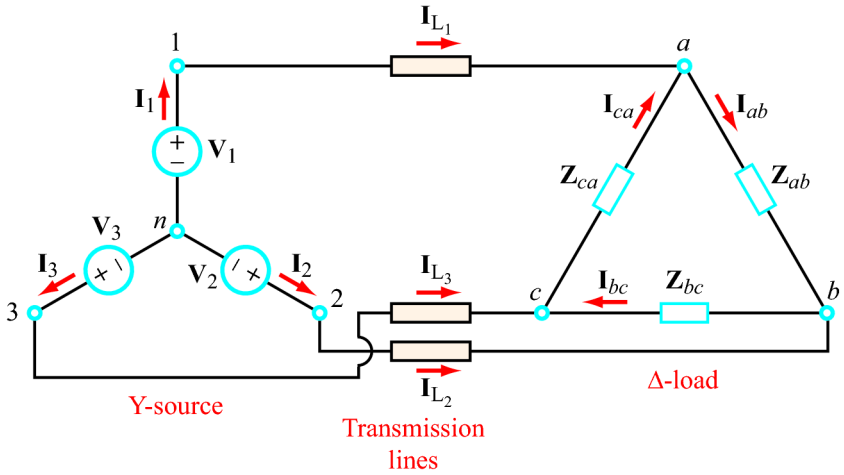
Figure 10.4 Y- and Δ-source configurations, with V_{Ys} = rms value of the phase-voltage magnitude of the Y-source. The rms magnitude of the Δ-source phase voltages is $\sqrt{3}\,V_{\text{Ys}}$.



(a) Y-Y configuration

Load Phase Currents
$\mathbf{I}_a$, $\mathbf{I}_b$, $\mathbf{I}_c$
(same as line currents $\mathbf{I}_{L_1}$, $\mathbf{I}_{L_2}$, and $\mathbf{I}_{L_3}$)

Load Phase Voltages
$\mathbf{V}_{aN}$, $\mathbf{V}_{bN}$, $\mathbf{V}_{cN}$

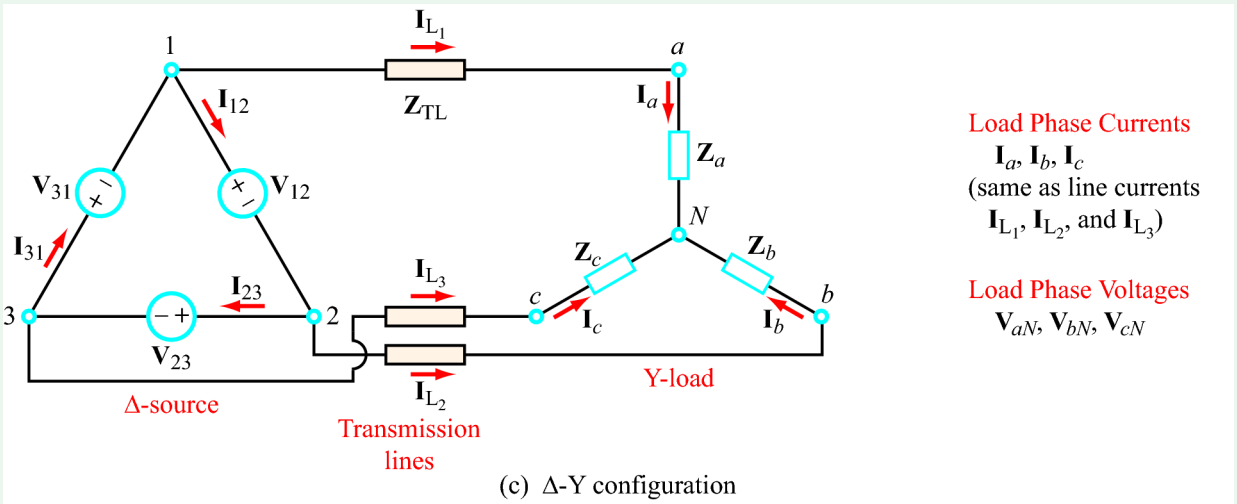


(b) Y-Δ configuration

Load Phase Currents
$\mathbf{I}_{ab}$, $\mathbf{I}_{bc}$, $\mathbf{I}_{ca}$

Load Phase Voltages
$\mathbf{V}_{ab}$, $\mathbf{V}_{bc}$, $\mathbf{V}_{ca}$

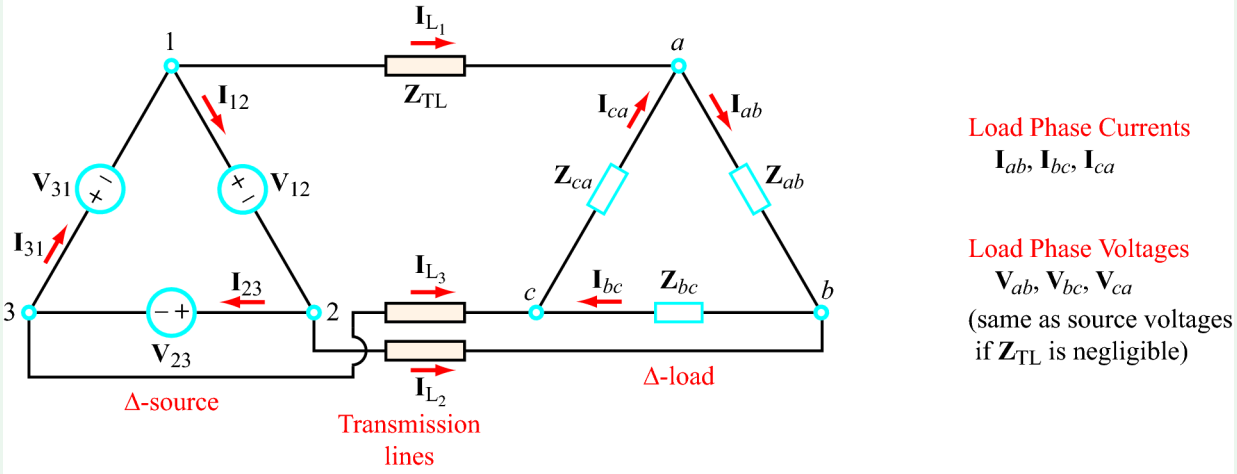
Figure 10.5 The three-phase source and load circuits can be connected in four possible arrangements: Y-Y, Y-Δ, Δ-Y, and Δ-Δ. In each arrangement, the source and load circuits are connected via transmission lines carrying ***line currents*** $\mathbf{I}_{L_1}$, $\mathbf{I}_{L_2}$, and $\mathbf{I}_{L_3}$. [Parts (c) and (d) follow on the next page.]



(c) Δ-Y configuration

Load Phase Currents
$\mathbf{I}_a$, $\mathbf{I}_b$, $\mathbf{I}_c$
(same as line currents $\mathbf{I}_{L_1}$, $\mathbf{I}_{L_2}$, and $\mathbf{I}_{L_3}$)

Load Phase Voltages
$\mathbf{V}_{aN}$, $\mathbf{V}_{bN}$, $\mathbf{V}_{cN}$



(d) Δ-Δ configuration

Load Phase Currents
$\mathbf{I}_{ab}$, $\mathbf{I}_{bc}$, $\mathbf{I}_{ca}$

Load Phase Voltages
$\mathbf{V}_{ab}$, $\mathbf{V}_{bc}$, $\mathbf{V}_{ca}$
(same as source voltages if $\mathbf{Z}_{TL}$ is negligible)

(**Fig. 10-5** continued)

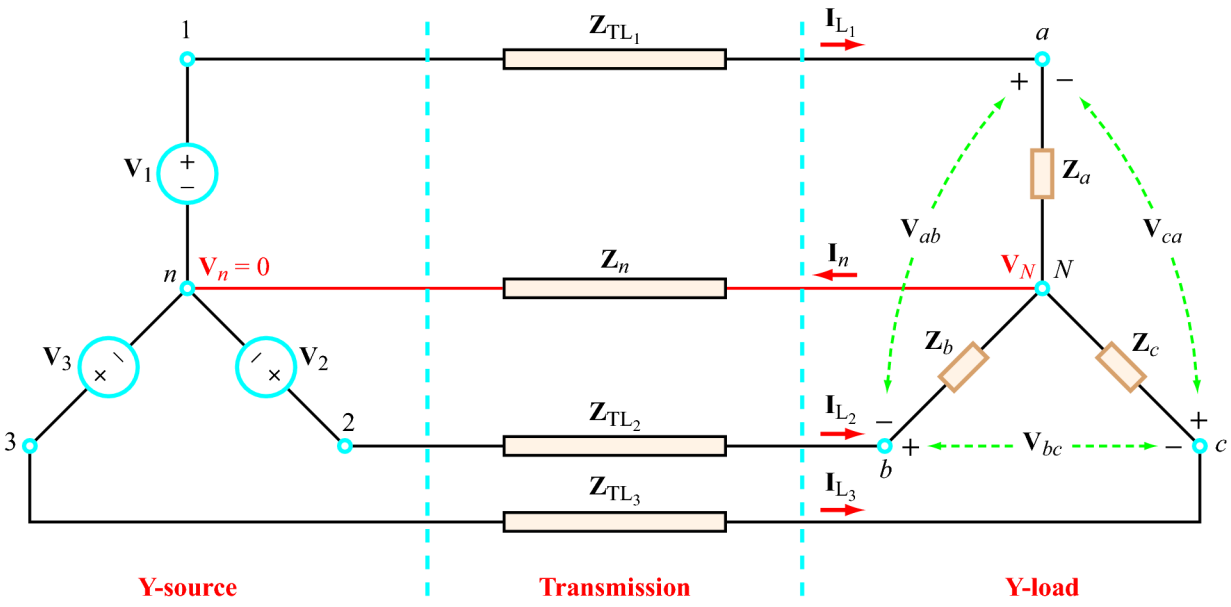


Figure 10.6 Three-phase Y source connected to a Y load circuit via transmission lines.

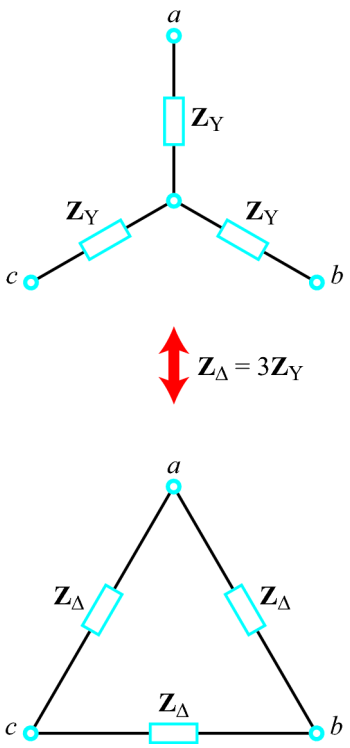


Figure 10.7 Y-Δ transformation for balanced load circuits.

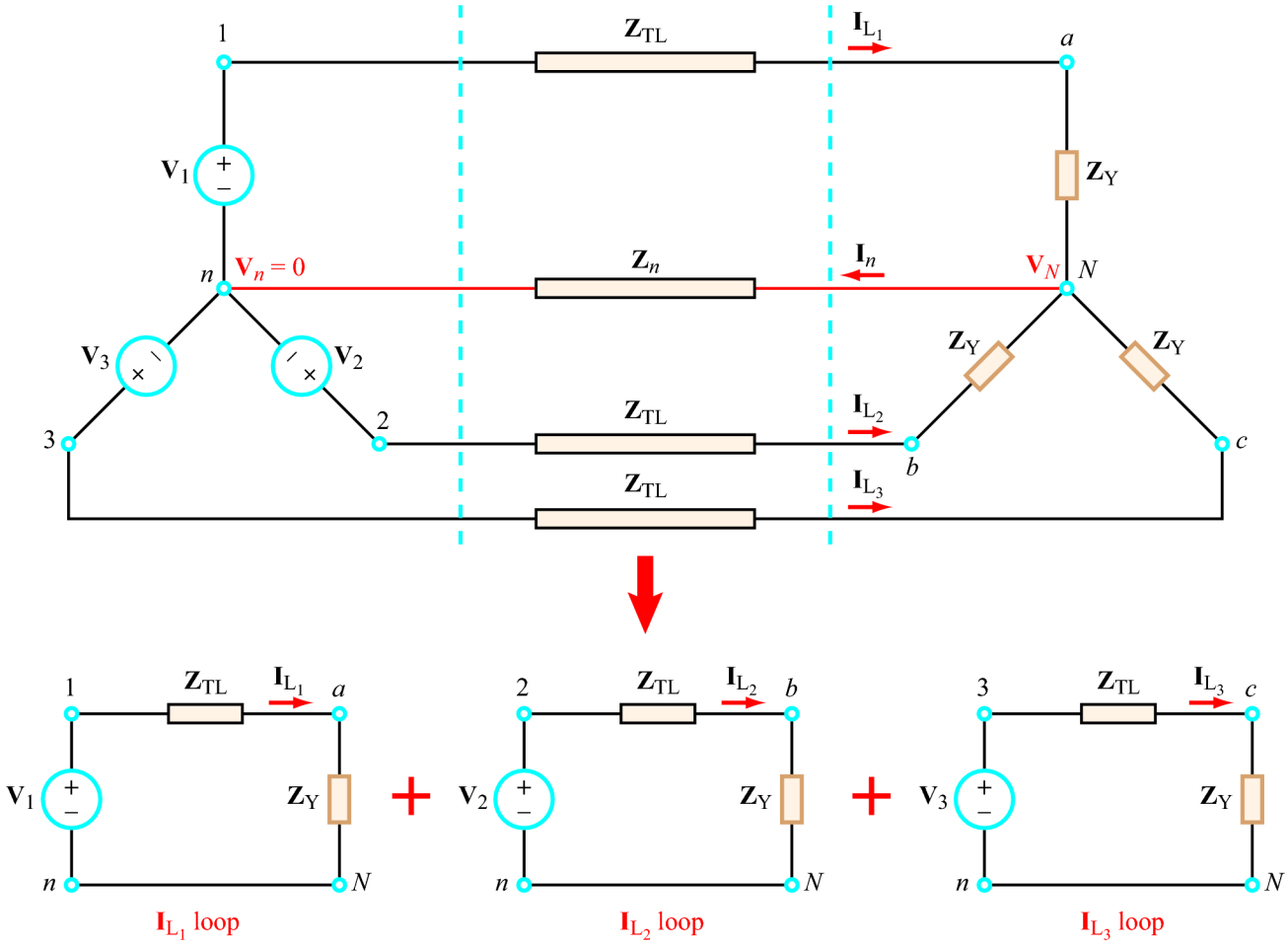
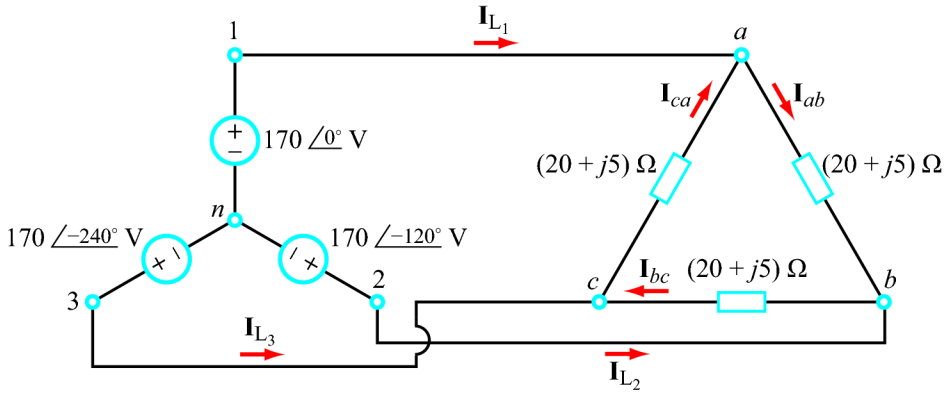
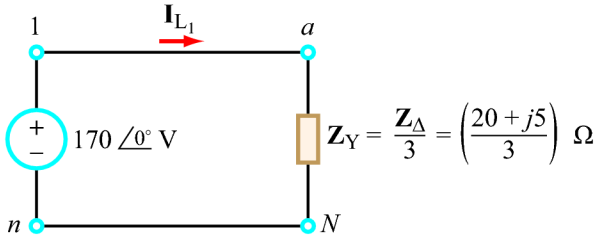


Figure 10.8 The balanced Y-Y network is equivalent to the sum of three, independent single-phase circuits.



(a) Y-Δ network



(b) Single-phase equivalent circuit

Figure 10.9 Circuit of Example 10-3 (voltage values are rms).

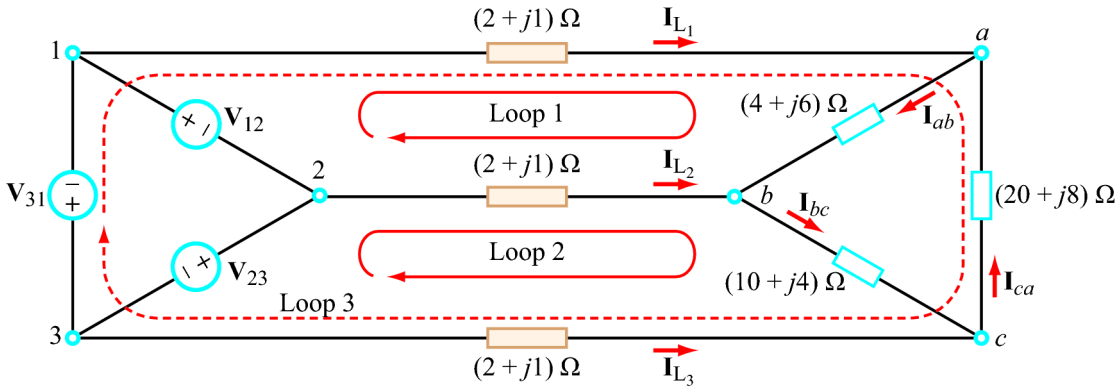


Figure 10.10 Δ-Δ network of Example 10-4.

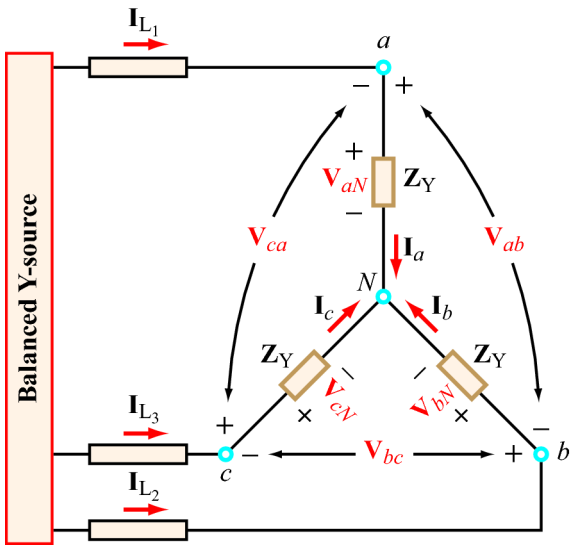


Figure 10.11 Balanced Y-load circuit with ***line voltages*** $\mathbf{V}_{ab}$ to $\mathbf{V}_{ca}$, ***line currents*** $\mathbf{I}_{L_1}$ to $\mathbf{I}_{L_3}$, ***phase voltages*** $\mathbf{V}_{aN}$ to $\mathbf{V}_{cN}$, and ***phase currents*** $\mathbf{I}_a$ to $\mathbf{I}_c$.

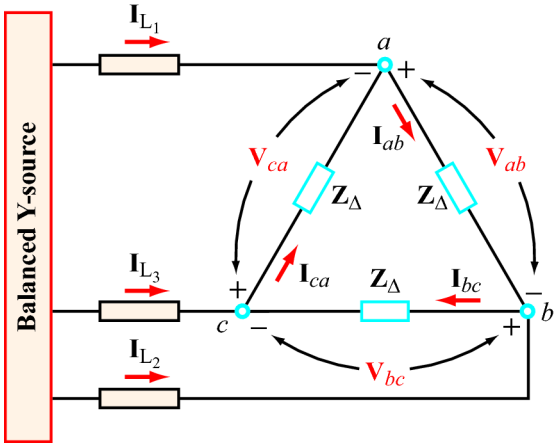
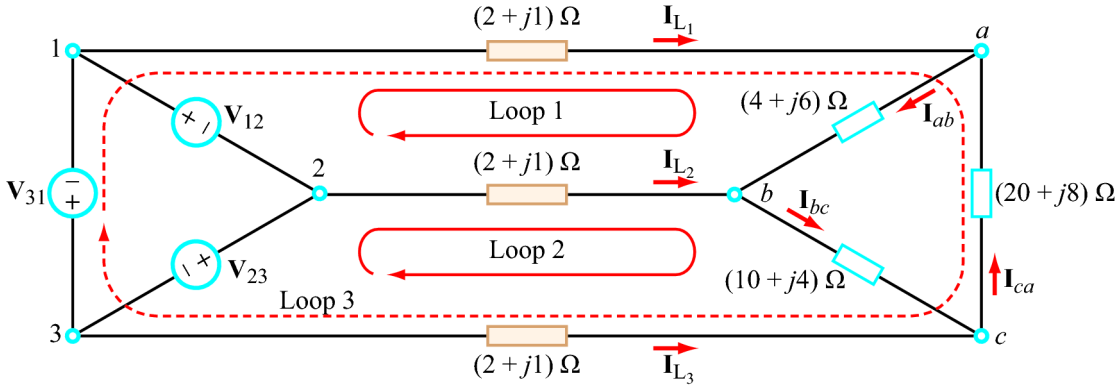
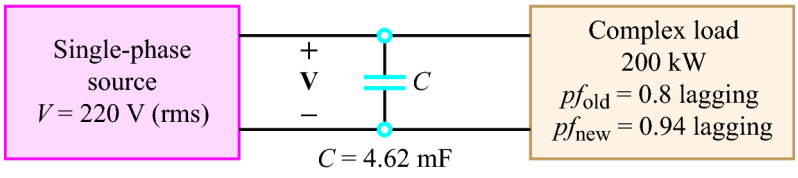


Figure 10.12 Balanced Δ-load circuit connected to a balanced Y-source.

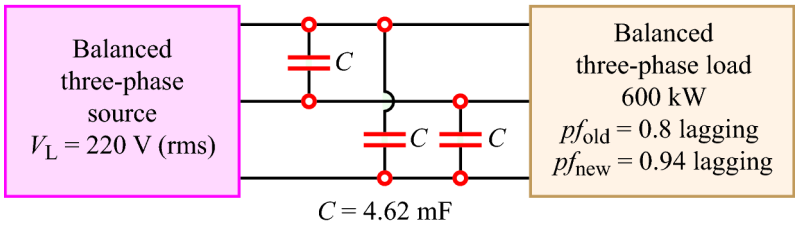


$\mathbf{I}_{L_1} = (44.56 + j1.23)$ A (rms)
$\mathbf{I}_{L_2} = (-26.94 - j31.32)$ A (rms)
$\mathbf{I}_{L_3} = (-17.63 - j30.09)$ A (rms)
$\mathbf{I}_{ab} = (33.31 + j5.95)$ A (rms)
$\mathbf{I}_{bc} = (6.38 - j25.37)$ A (rms)
$\mathbf{I}_{ca} = (-11.25 + j4.72)$ A (rms)

Figure 10.13 Circuit of Example 10-4 with calculated values of the currents.

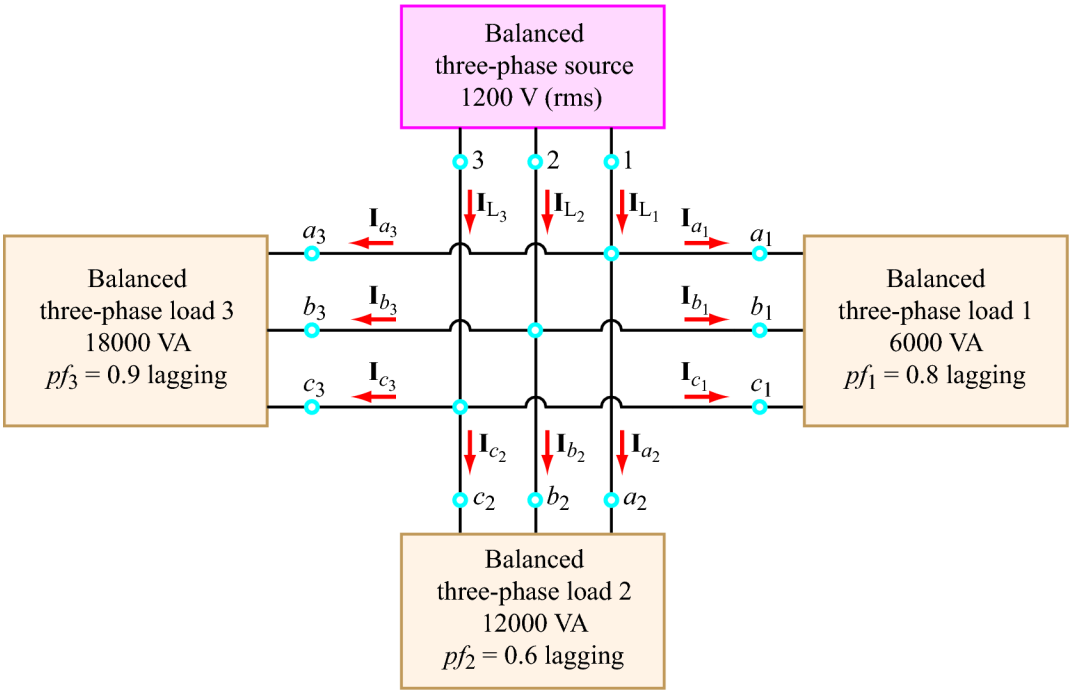


(a) Single-phase

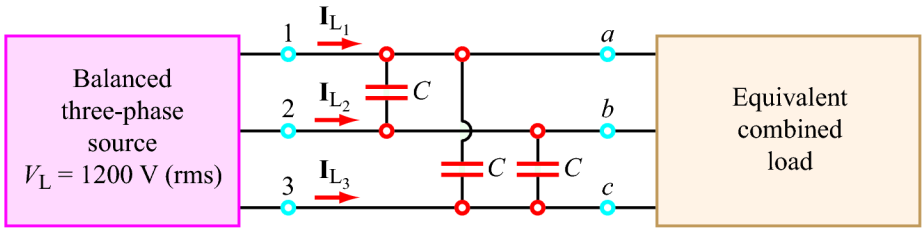


(b) Three-phase

Figure 10.14 A balanced three-phase load can be compensated by treating it as three individual circuits each consuming one-third of the total power.

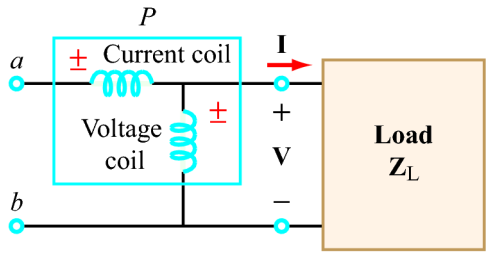


(a) Original circuit

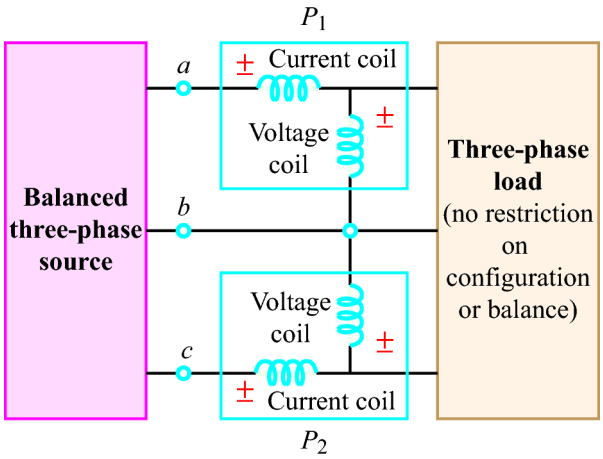


(b) Equivalent circuit with shunt capacitors added

Figure 10.15 Three-phase source connected in parallel to three loads, each a balanced three-phase load (Example 10-7).



(a) Single-phase power measurement



(b) Three-phase power measurement

Figure 10.16 A wattmeter uses two coils. The double polarity mark (±) of the current coil denotes the terminal that should be toward the source, and on the voltage coil, ± marks the terminal that should be connected to the line containing the current coil.

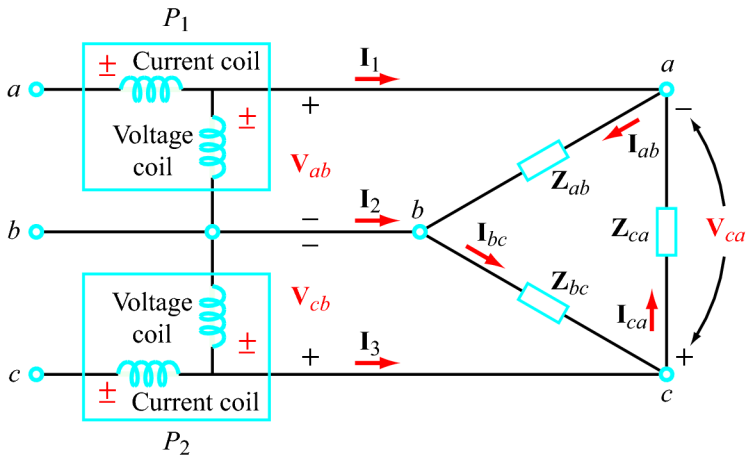
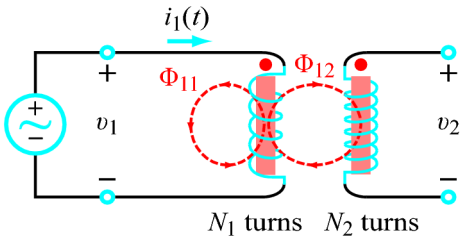
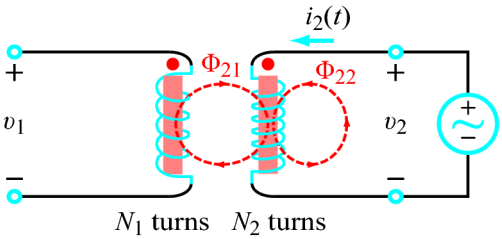


Figure 10.17 Two-wattmeter method applied to an unbalanced Δ-load.



(a) Current i_1 induces Φ_{11} and Φ_{12}, which induces v_2



(b) Current i_2 induces Φ_{22} and Φ_{21}, which induces v_1

Figure 11.1 Magnetically coupled coils.

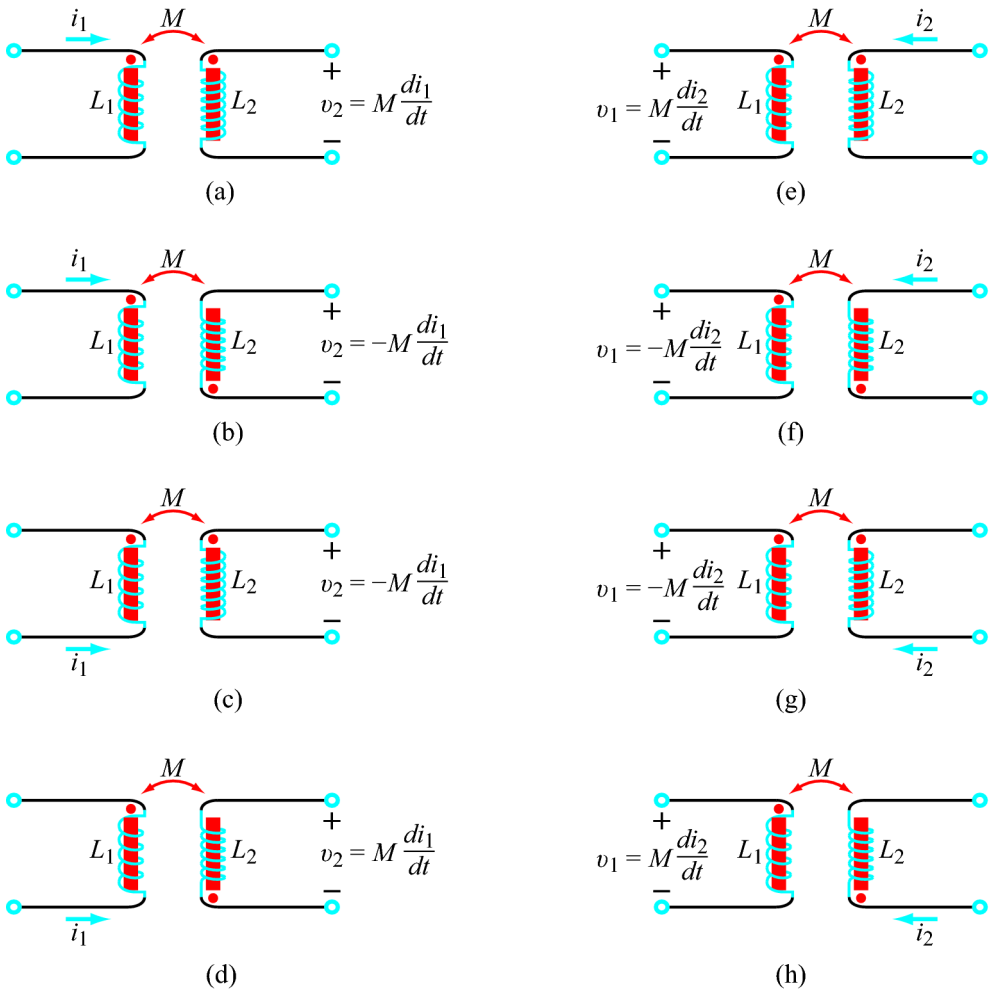
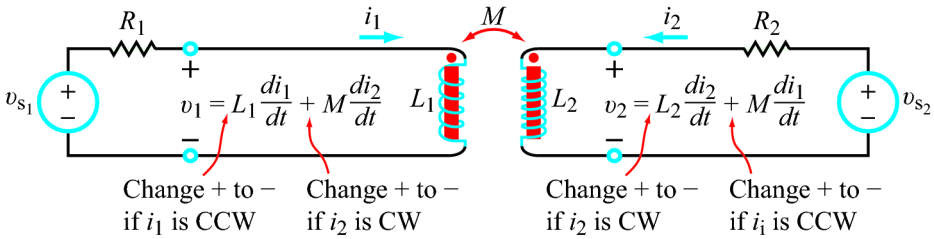
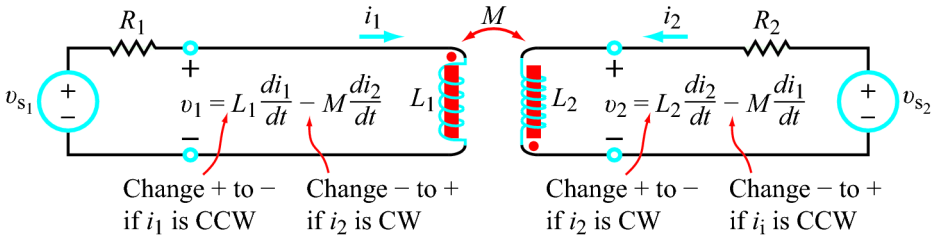


Figure 11.2 Dot convention for the mutual-inductance voltage induced in coil 2 by current i_1 in coil 1, and vice versa.

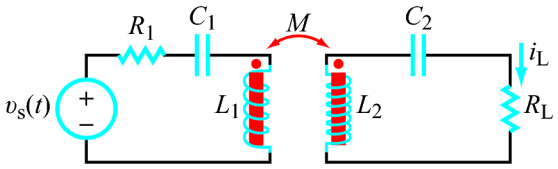


(a) Dots on same ends

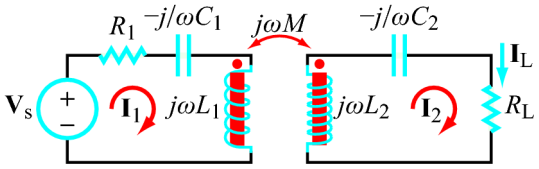


(b) Dots on opposite ends

Figure 11.3 Polarities of voltage components for clockwise (CW) and counterclockwise (CCW) current directions.



(a) Time domain



(b) Phasor domain

Figure 11.4 Circuit of Example 11-1.

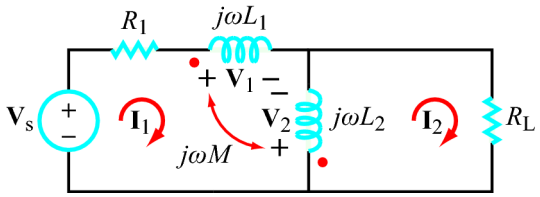


Figure 11.5 Circuit of Example 11-2.

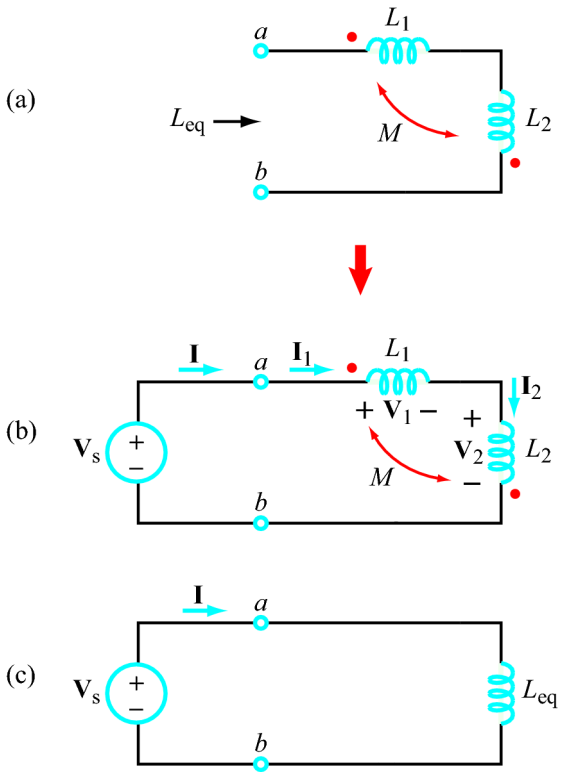
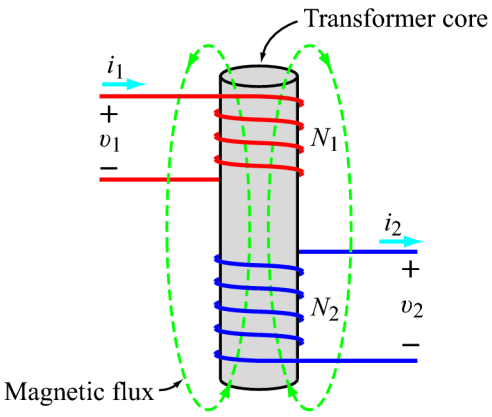
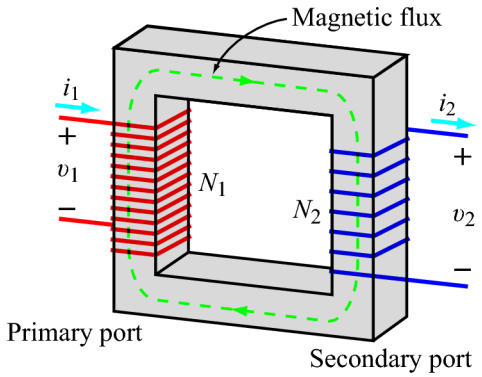


Figure 11.6 Finding L_{eq} of two series-coupled inductors (Example 11-3).

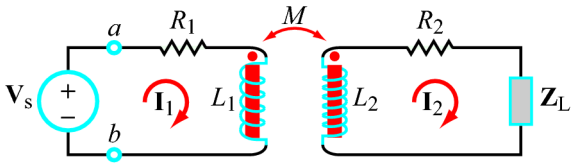


(a) Cylindrical core

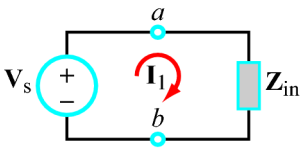


(b) Rectangular core

Figure 11.7 Magnetically coupled coils.



(a) Original circuit



(b) Equivalent circuit

Figure 11.8 (a) Transformer circuit with coil resistors R_1 and R_2, and (b) in terms of an equivalent input impedance $\mathbf{Z}_{in}$.

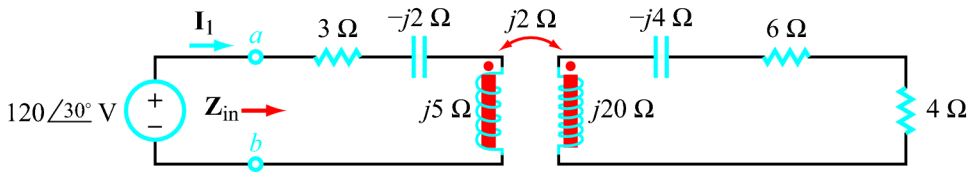


Figure 11.9 Circuit of Example 11-4.

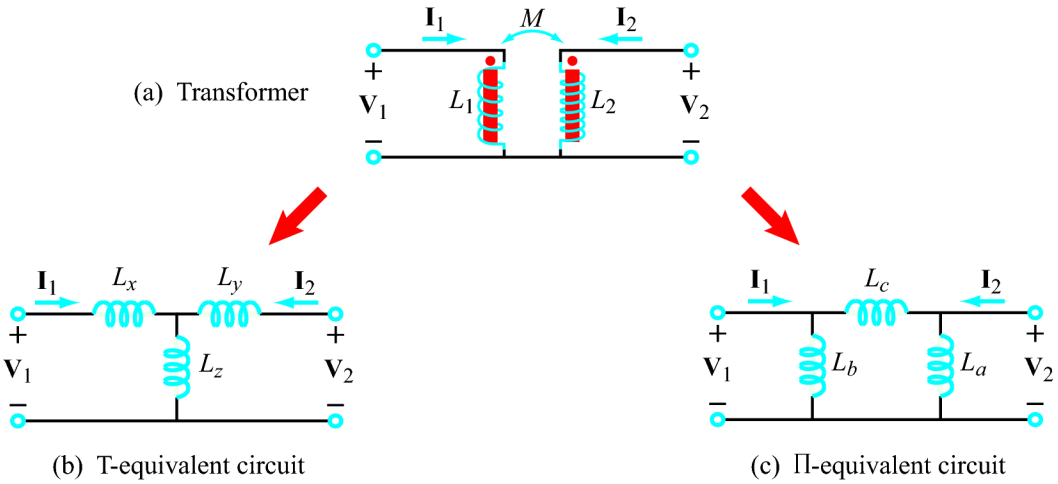
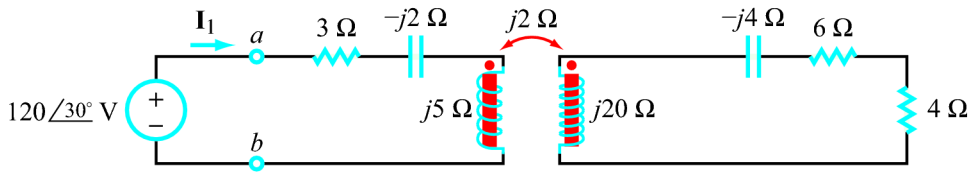
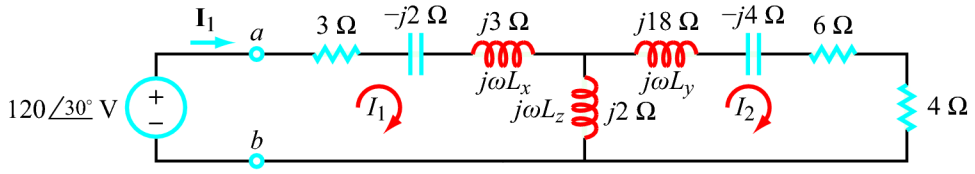


Figure 11.10 The transformer can be modeled in terms of T- or Π-equivalent circuits.



(a) Original circuit



(b) Equivalent circuit

Figure 11.11 (a) Original circuit and (b) after replacing transformer with T-equivalent circuit.

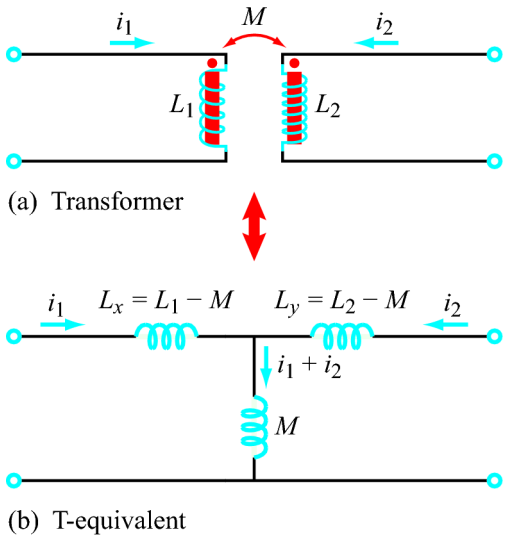


Figure 11.12 Transformer and its T-equivalent circuit. Reversing the direction of either current or if dots are on opposite ends, M should be replaced with $-M$.

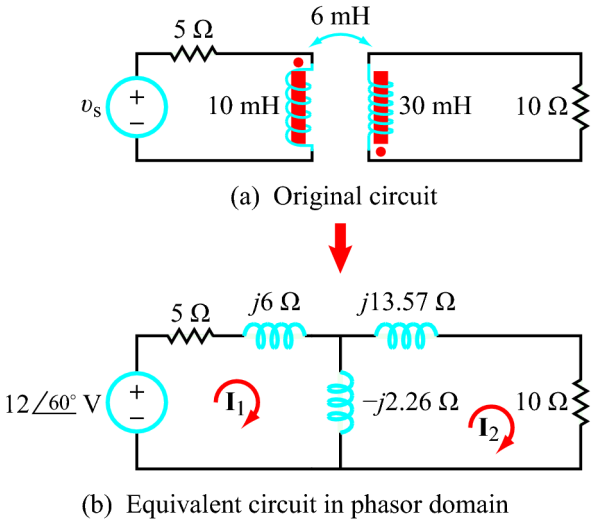
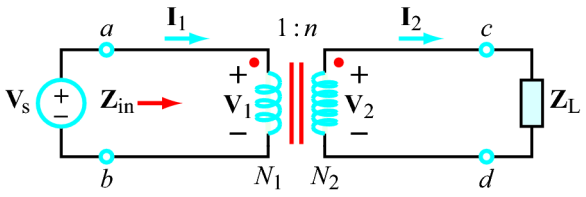
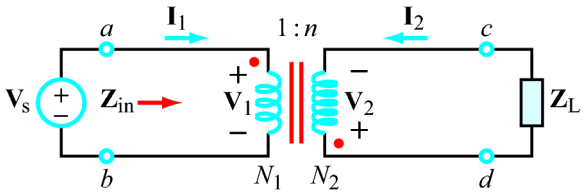


Figure 11.13 Circuits of Example 11-6.

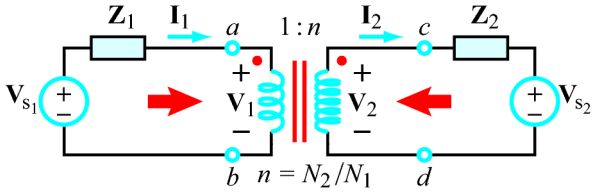


(a) Dots on same ends

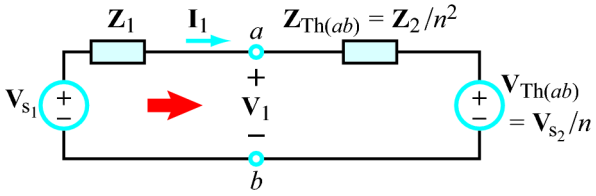


(b) Dots on opposite ends

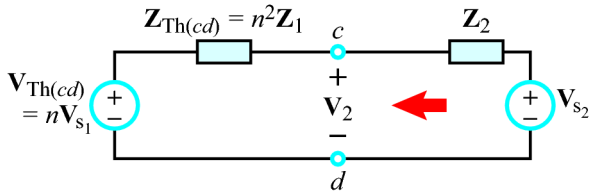
Figure 11.14 Schematic symbol for an ideal transformer. Note the reversal of the voltage polarity and current direction when the dot location at the secondary is moved from the top end of the coil to the bottom end. For both configurations: $\mathbf{V}_2/\mathbf{V}_1 = N_2/N_1 = n$, $\mathbf{I}_2/\mathbf{I}_1 = N_1/N_2 = 1/n$.



(a) Original circuit

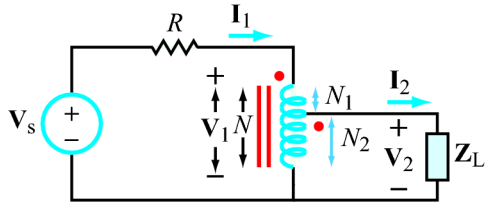


(b) Thévenin equivalent of circuit to the right of terminals (a, b)

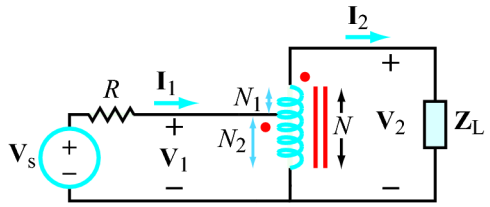


(c) Thévenin equivalent of circuit to the left of terminals (c, d)

Figure 11.15 Thévenin equivalent circuit of Example 11-7.

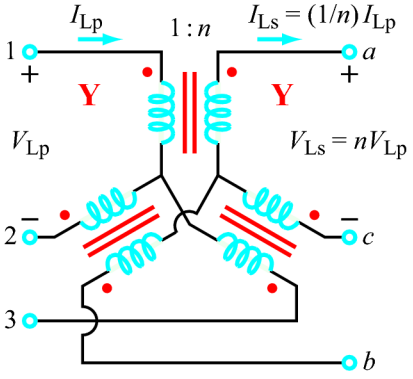


(a) Step-down autotransformer

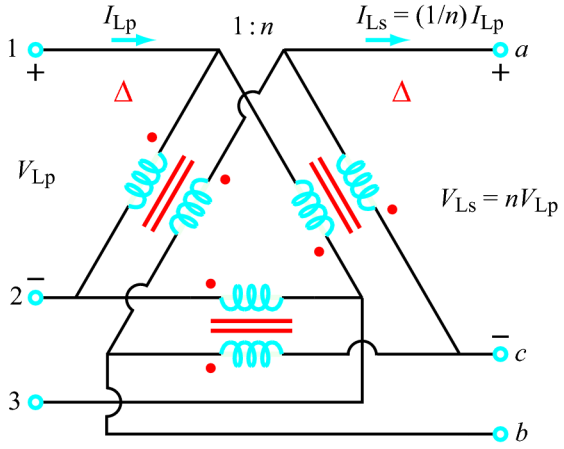


(b) Step-up autotransformer

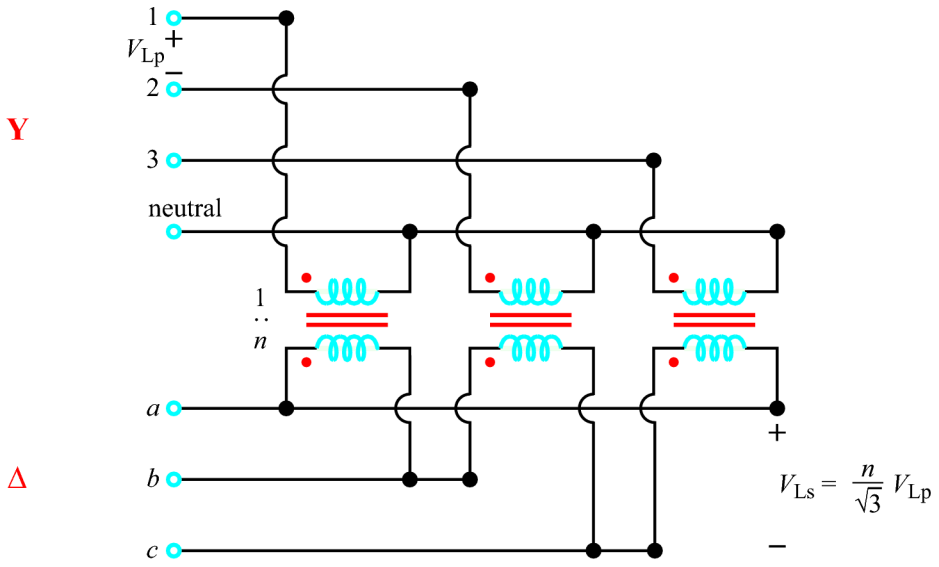
Figure 11.16 Autotransformer circuits.



(a) Y-Y transformer



(b) Δ-Δ transformer



(c) Y-Δ transformer

Figure 11.17 Three possible connection configurations for three-phase transformers.

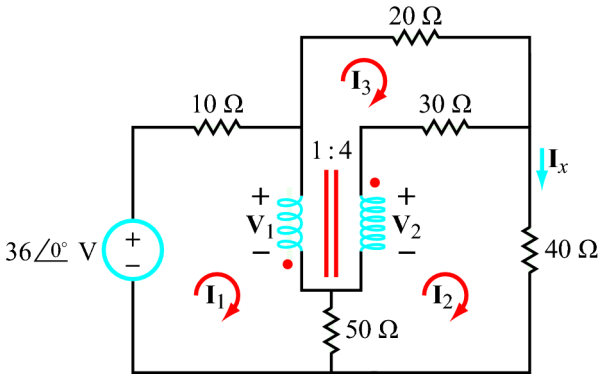
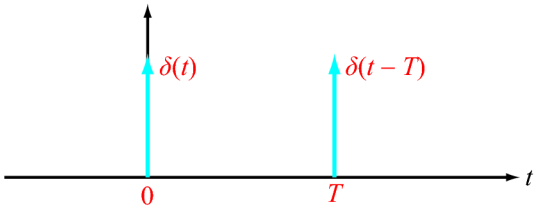
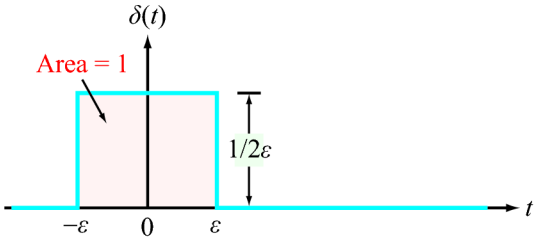


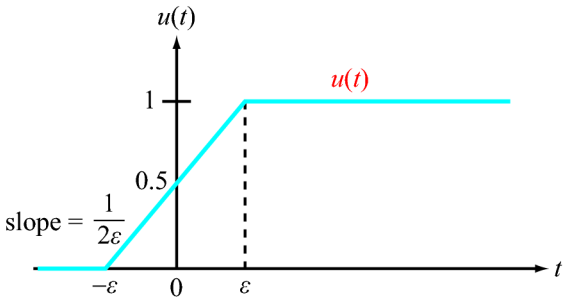
Figure 11.18 Circuit of Example 11-10.



(a) $\delta(t)$ and $\delta(t - T)$



(b) Rectangle model



(c) Gradual step model

Figure 12.1 Unit impulse function.

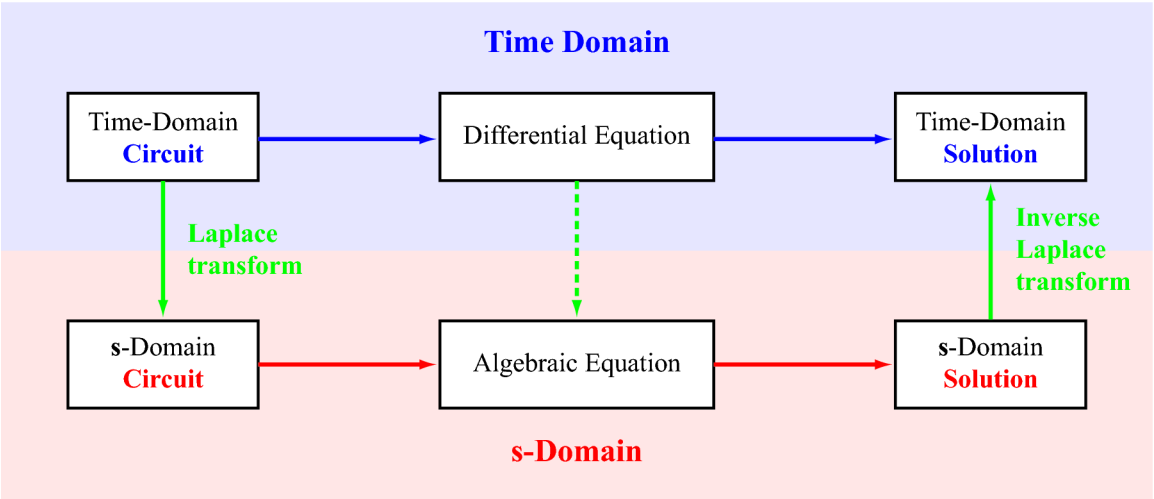


Figure 12.2 The top horizontal sequence involves solving a differential equation entirely in the time domain. The bottom horizontal sequence involves a much easier solution of a linear equation in the **s**-domain.

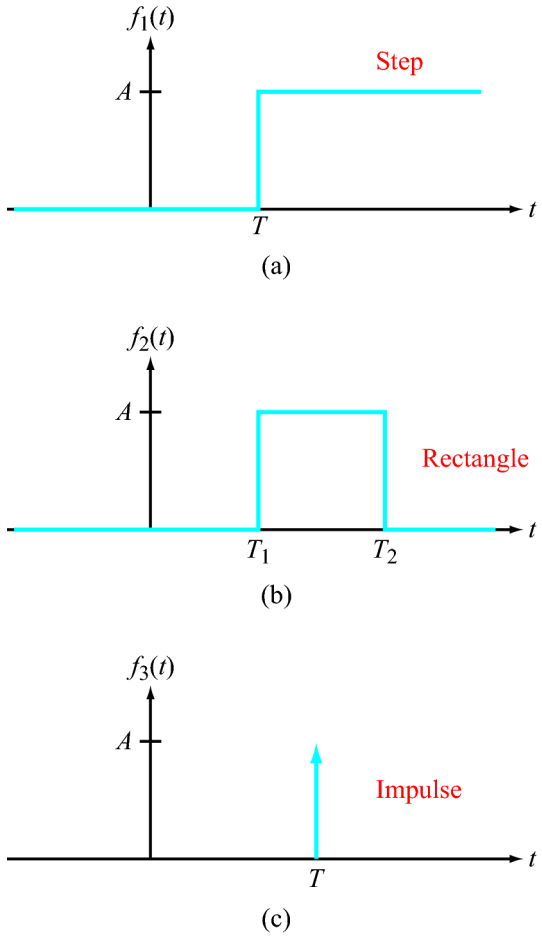
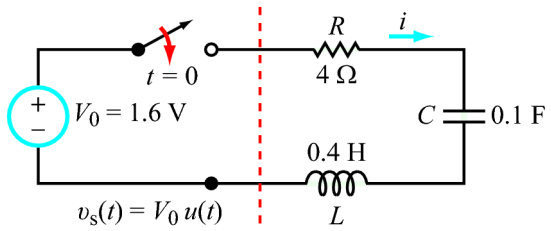
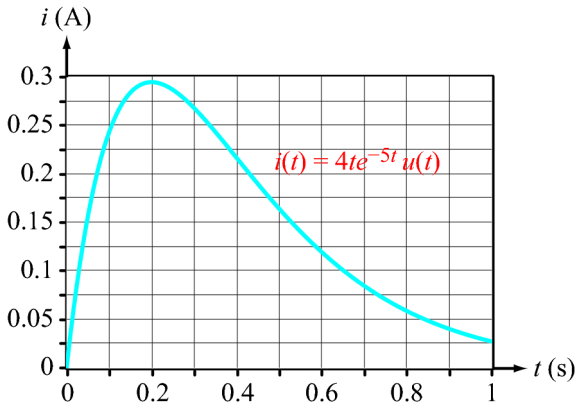


Figure 12.3 Singularity functions for Example 12-1.

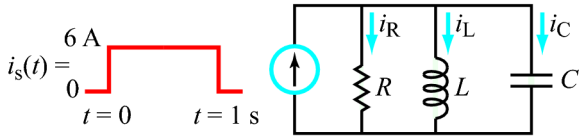


(a) RLC circuit

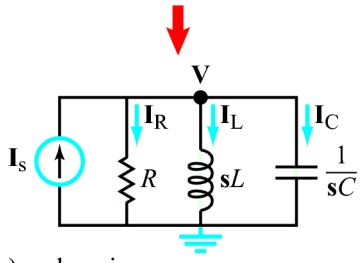


(b) $i(t)$

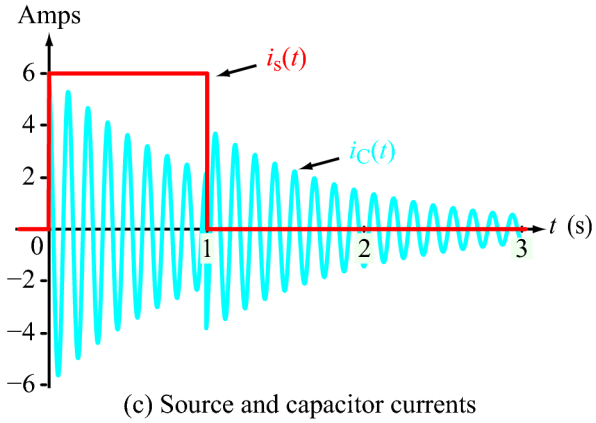
Figure 12.4 The dc source, in combination with the switch, constitutes an input excitation $v_s(t) = V_o\, u(t)$.



(a) RLC circuit in time domain

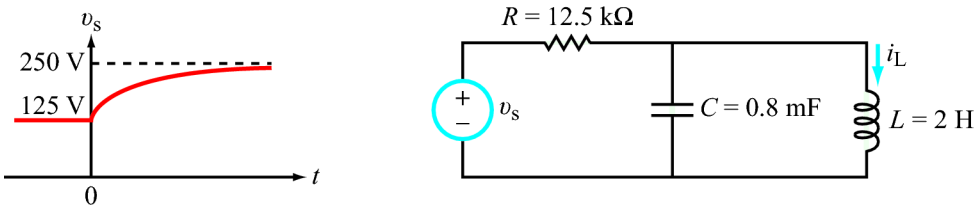


(b) **s**-domain

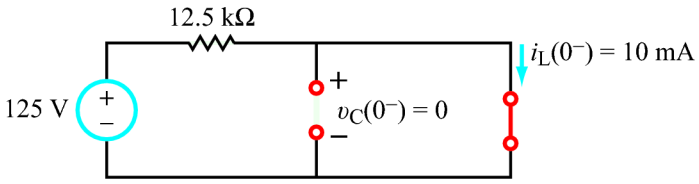


(c) Source and capacitor currents

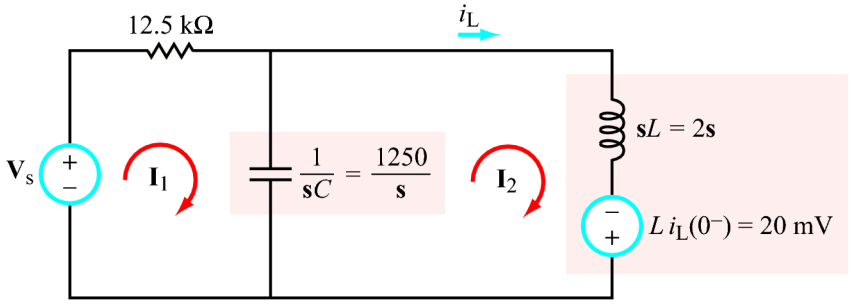
Figure 12.5 Circuit for Example 12-6.



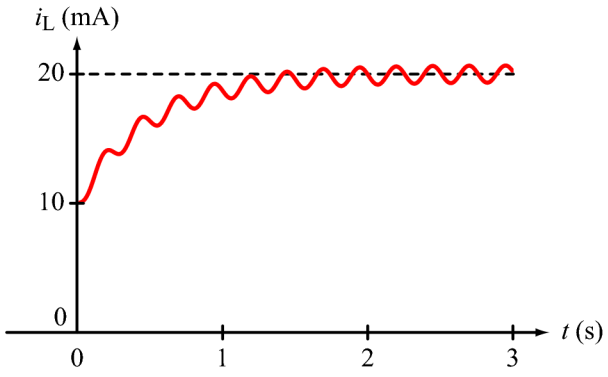
(a) Circuit



(b) Circuit at $t < 0$

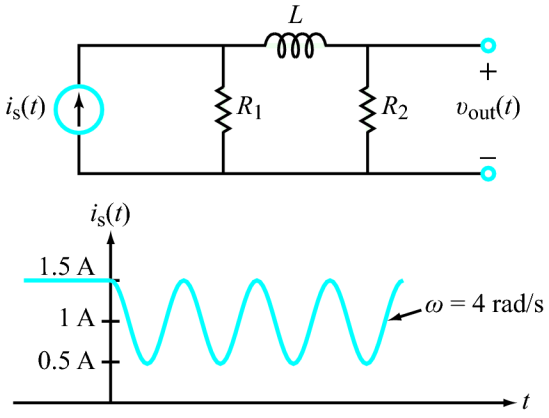


(c) **s**-domain for $t \geq 0$

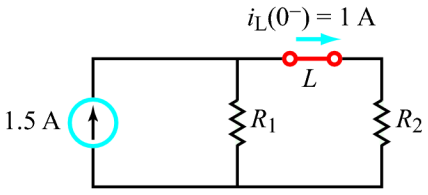


(d) $i_L(t)$

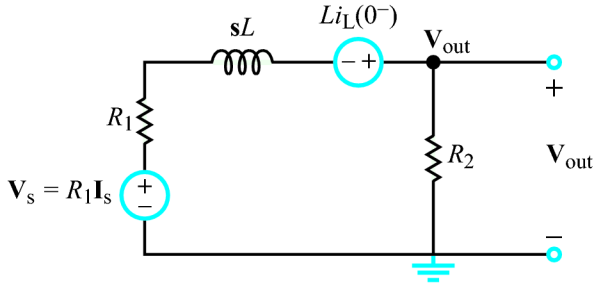
Figure 12.6 Example 12-7.



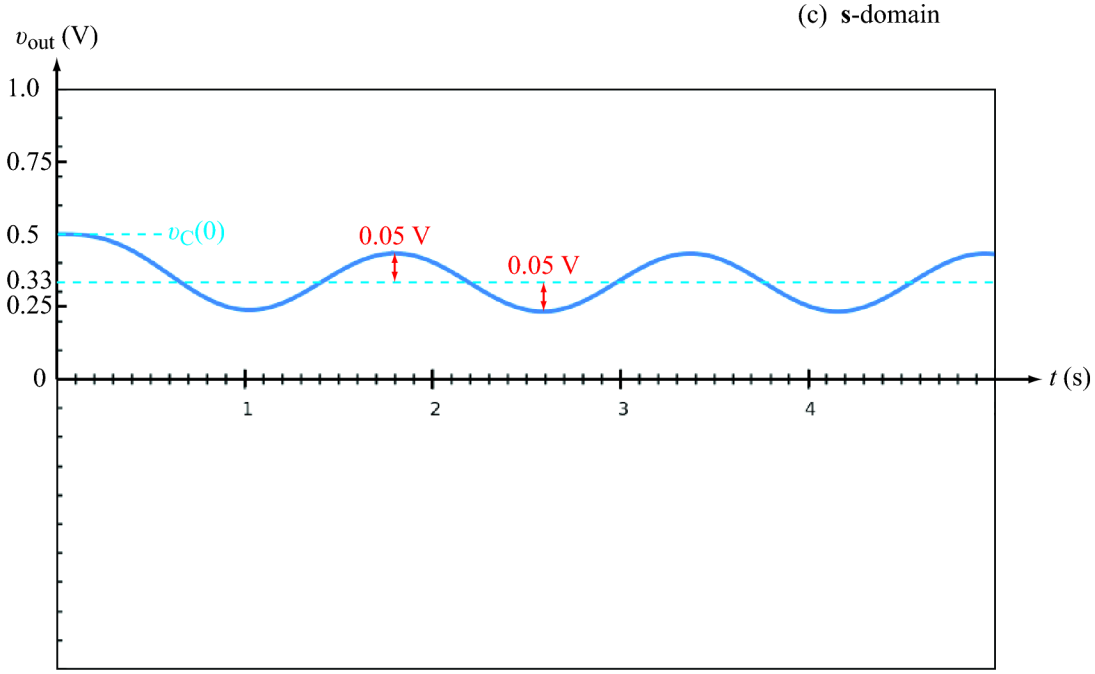
(a) Circuit and source waveform



(b) At $t = 0^-$



(c) **s**-domain



(d) $v_C(t)$

Figure 12.7 Example 12-8.

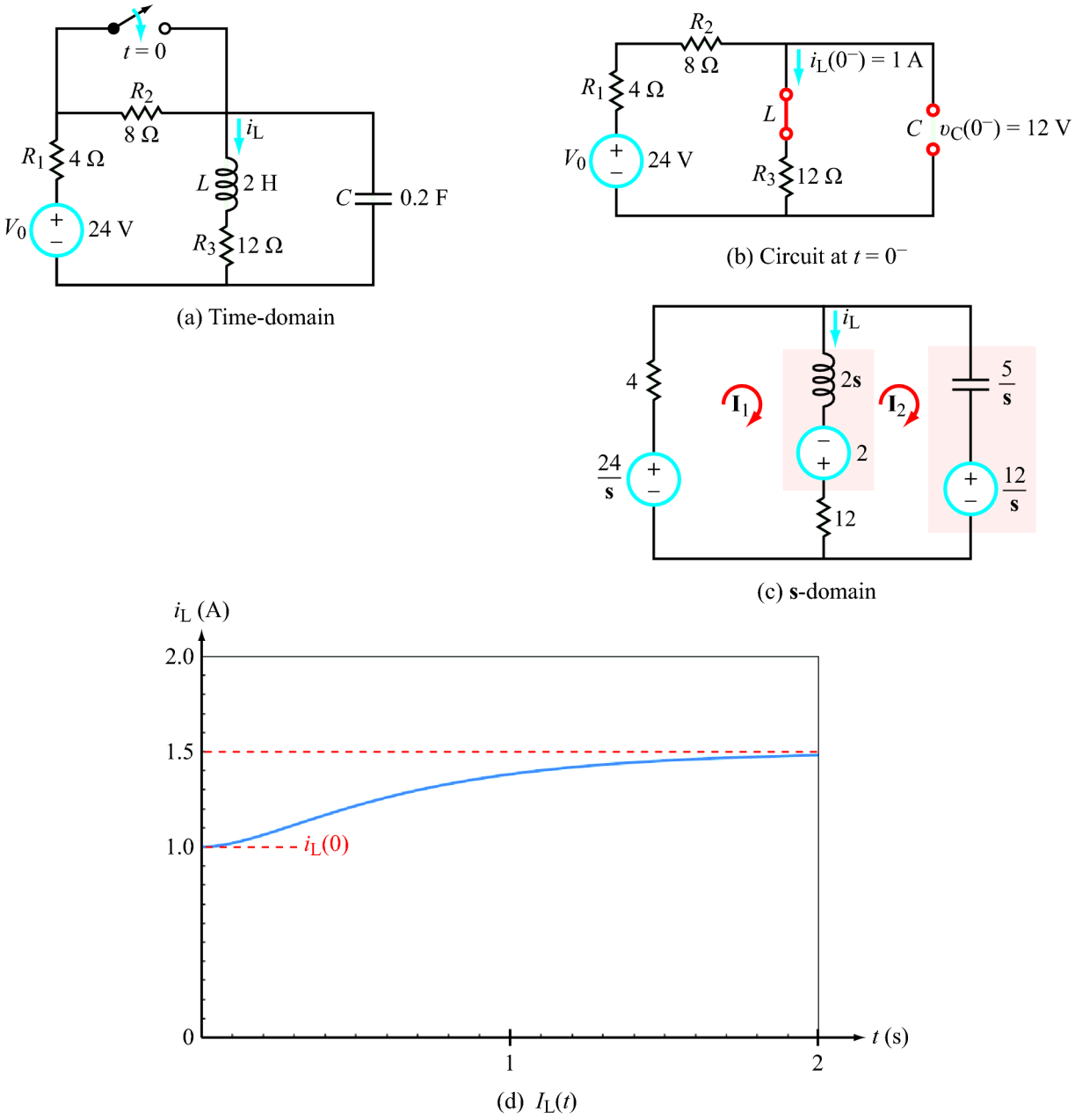
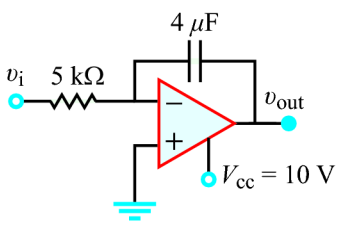
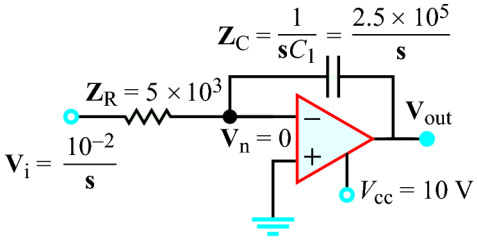


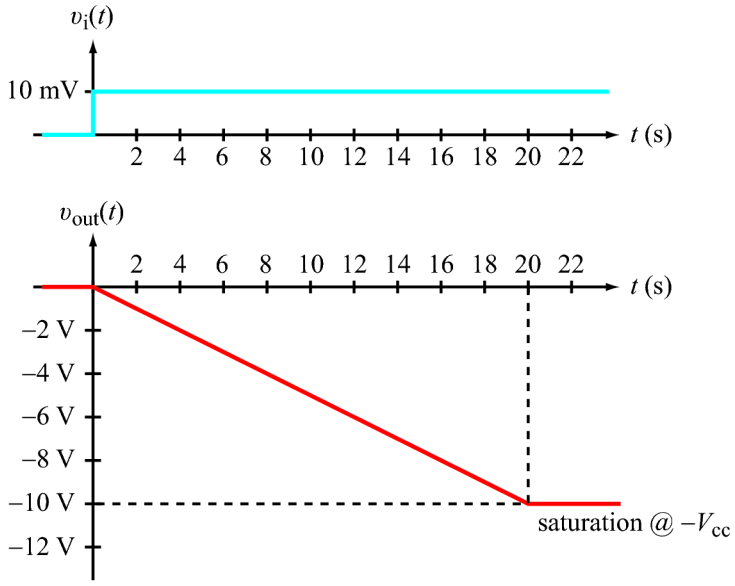
Figure 12.8 Circuit for Example 12-9.



(a) Circuit

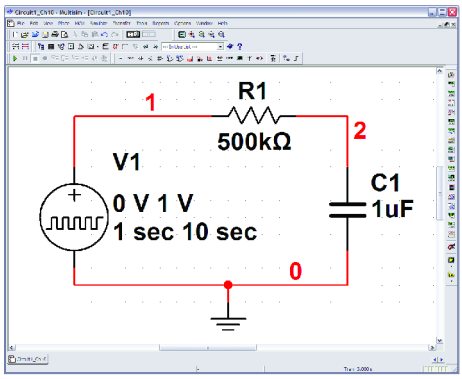


(b) **s**-domain

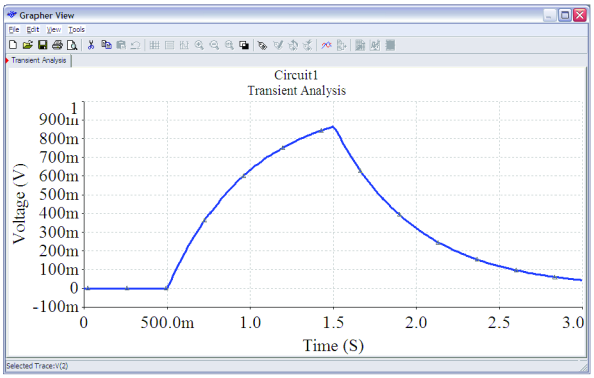


(c) $v_i(t)$ and $v_{out}(t)$

Figure 12.9 Circuit for Example 12-10.

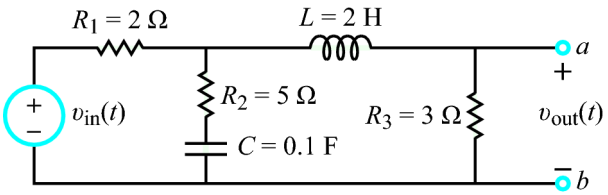


(a) Circuit in Multisim

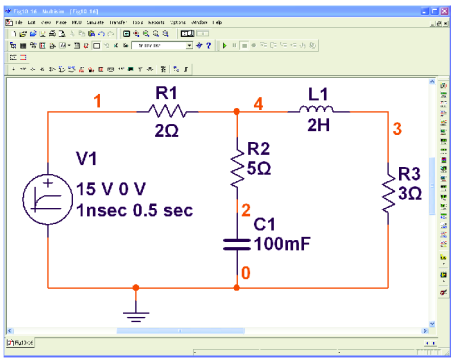


(b) Response

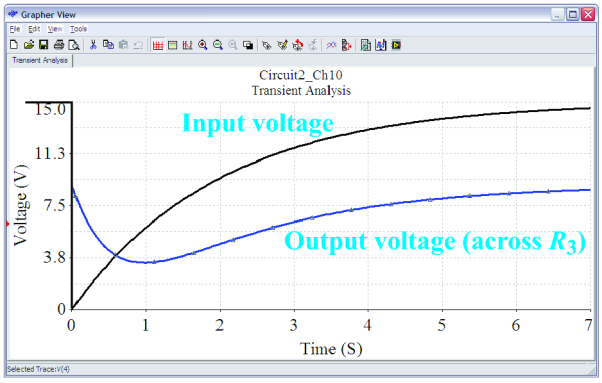
Figure 12.10 (a) RC circuit excited by a 1 V, 1 s rectangular pulse at 0.5 s, and (b) the corresponding response at node 2.



(a) Time domain

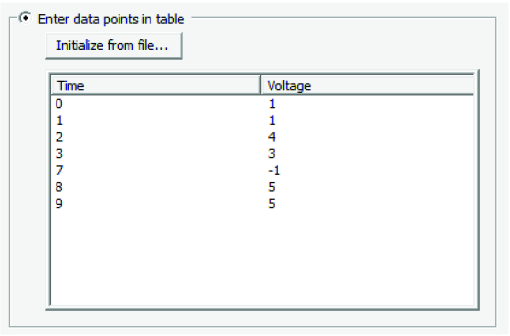


(b) Circuit in Multisim

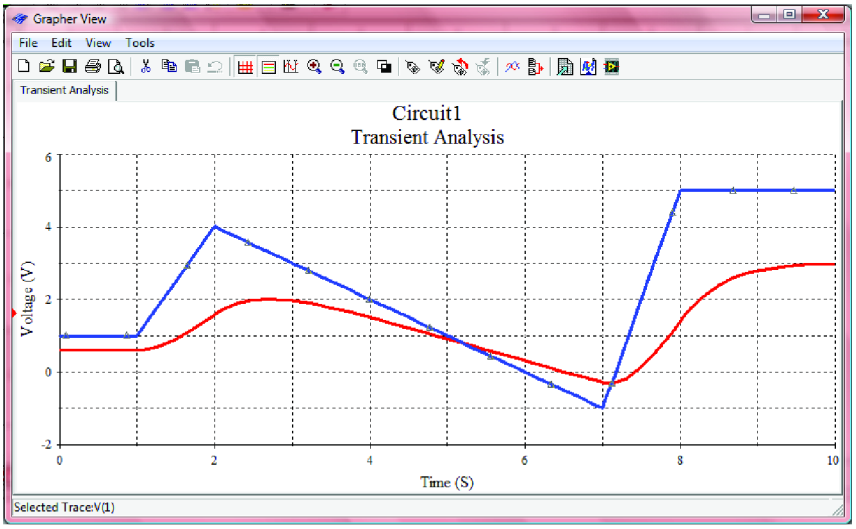


(c) Response

Figure 12.11 Multisim rendition of the circuit response to a sudden (but temporary) change in supply voltage level.



(a) Time-voltage pairs for circuit



(b) Response

Figure 12.12 Multisim rendition of the circuit response to an arbitrary input signal produced by the PWL (Piecewise Linear) source.

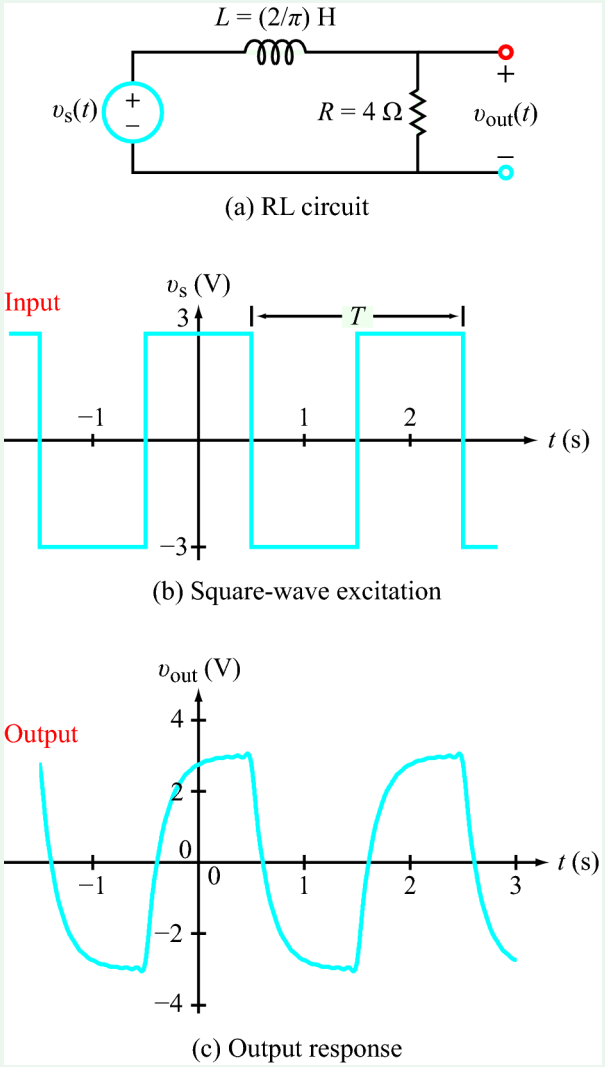


Figure 13.1 RL circuit excited by a square wave and corresponding output response.

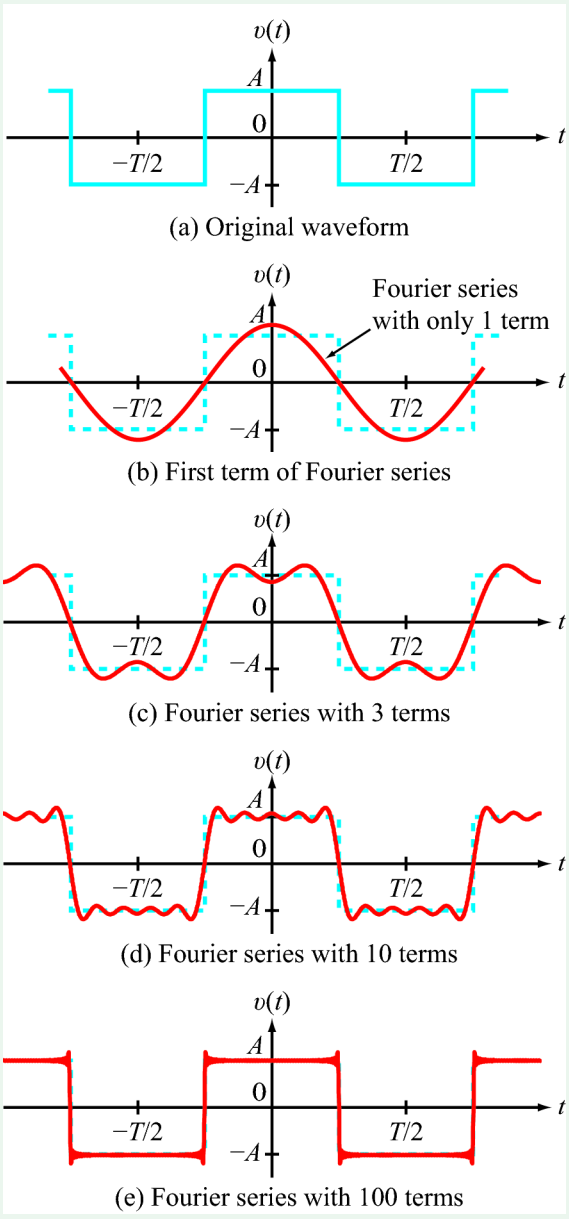


Figure 13.2 Comparison of the square-wave waveform with its Fourier series representation using only the first term (b), the sum of the first three (c), ten (d), and 100 terms (e).

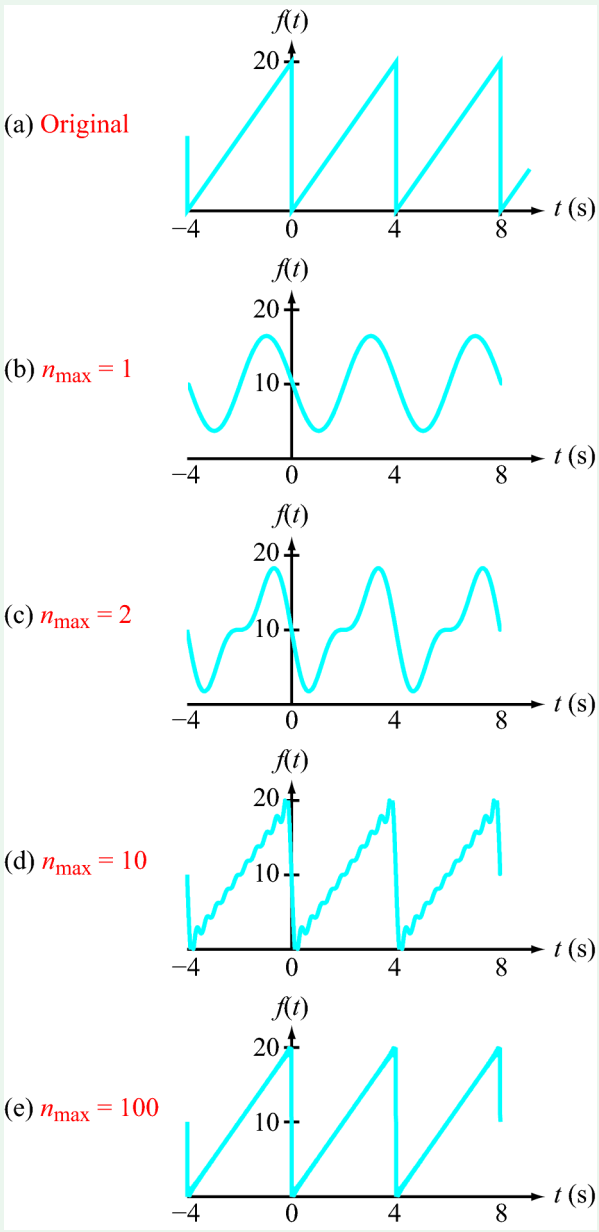


Figure 13.3 Sawtooth waveform: (a) original waveform, (b)–(e) representation by a truncated Fourier series with $n_{max} = 1$, 2, 10, and 100, respectively.

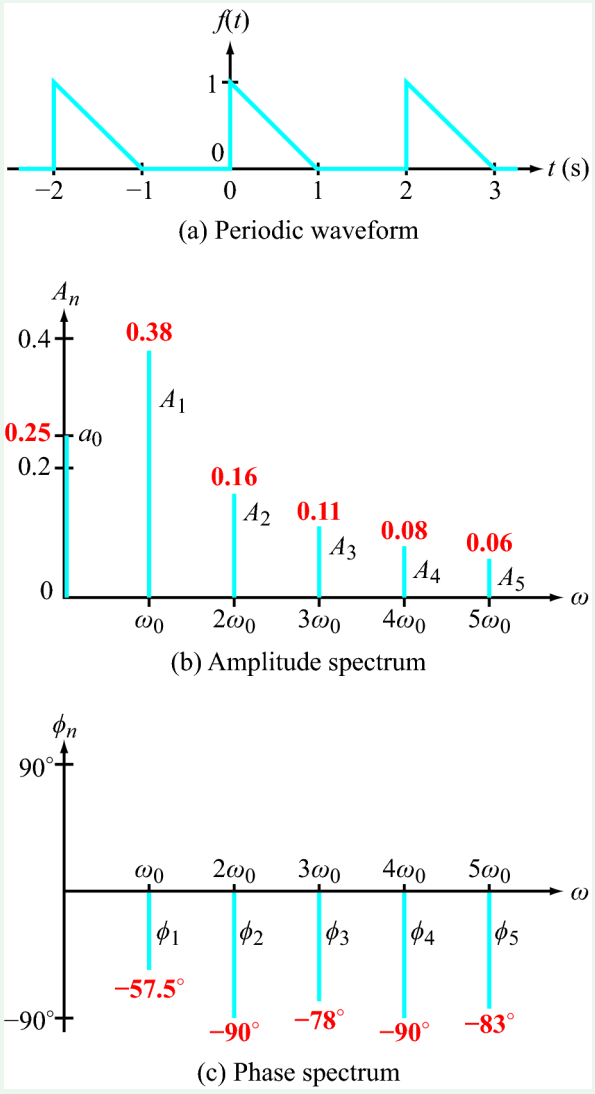


Figure 13.4 Periodic waveform of Example 13-2 with its associated line spectra.

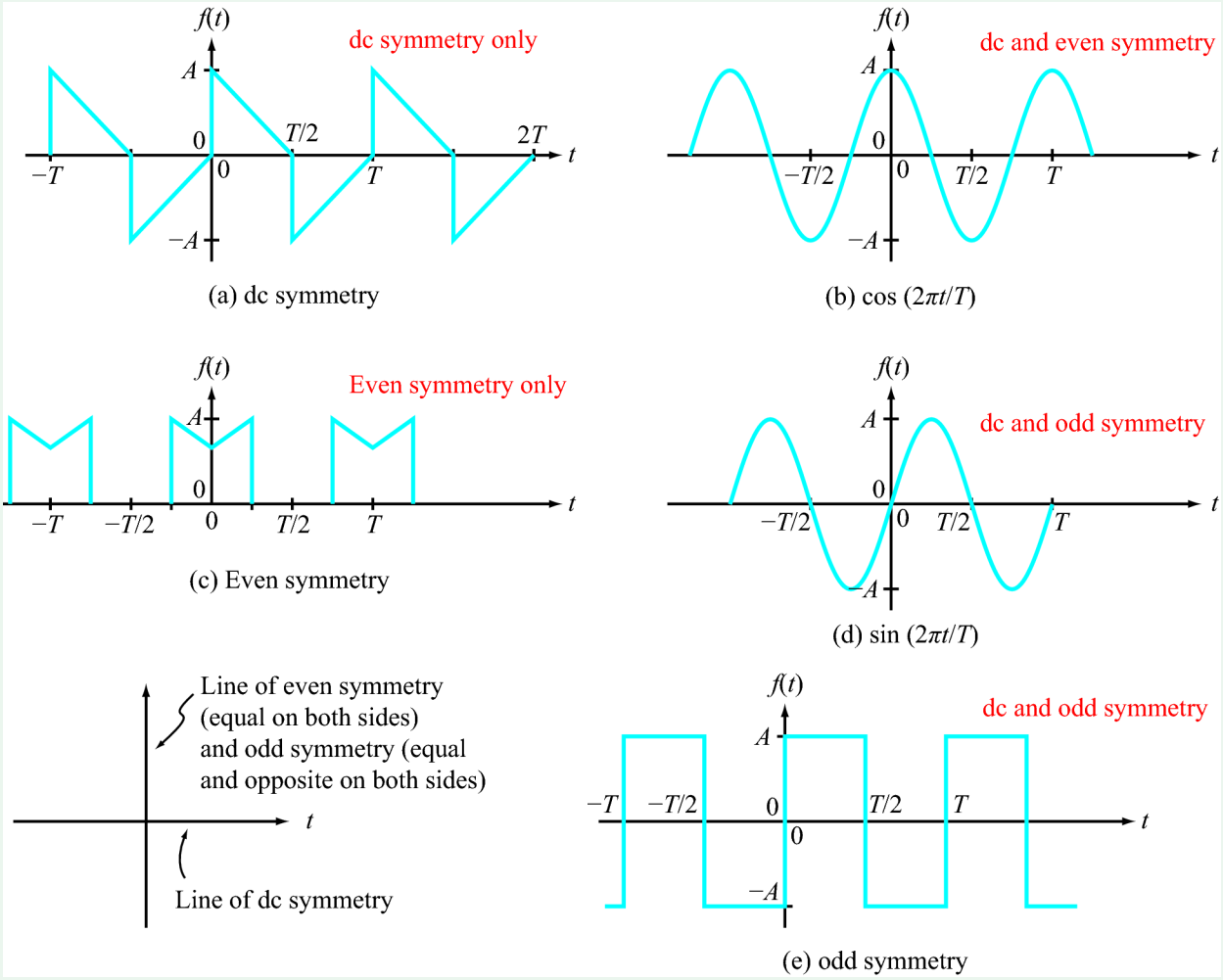


Figure 13.5 Waveforms with (a) dc symmetry, (b and c) even symmetry, and (d and e) odd symmetry.

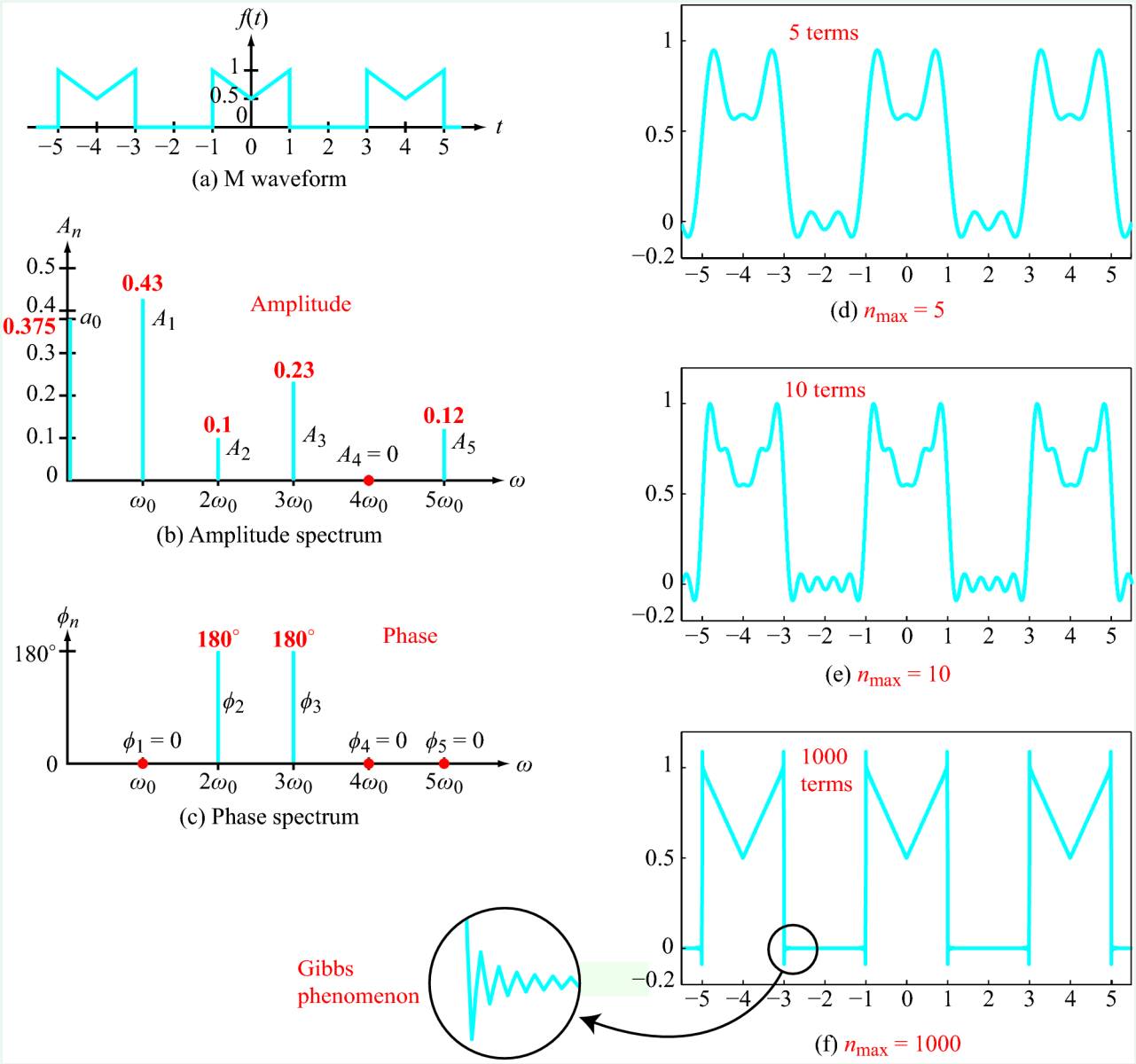


Figure 13.6 Plots for Example 13-3.

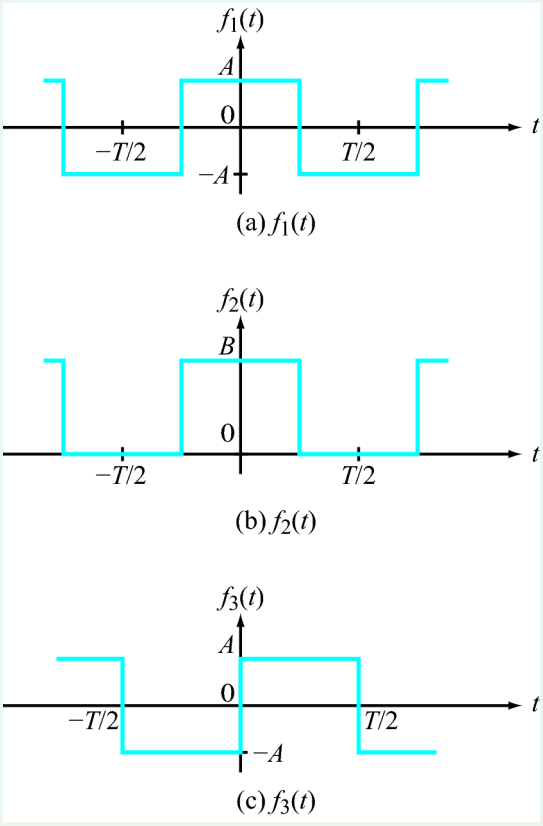


Figure 13.7 Waveforms for Example 13-4.

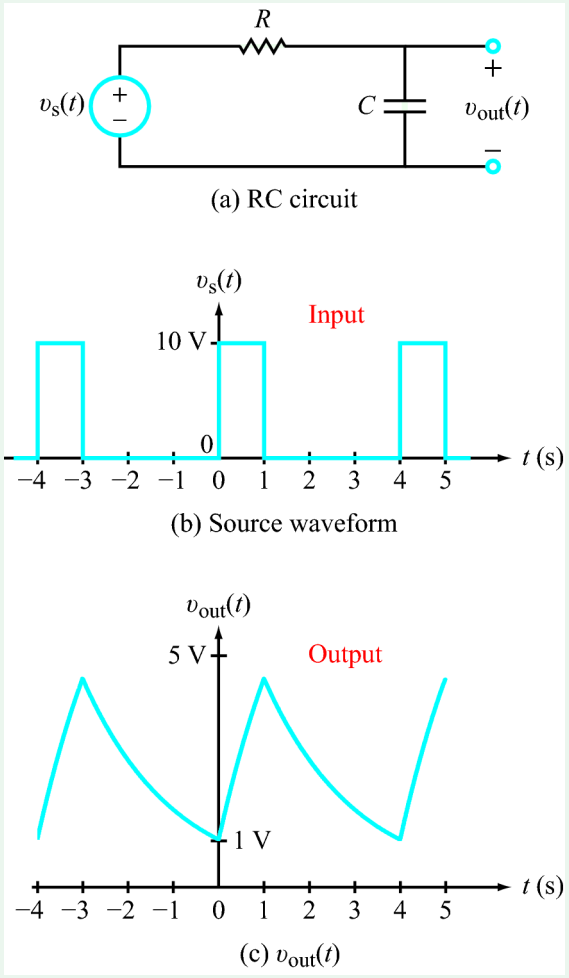


Figure 13.8 Circuit response to periodic pulses (Example 13-5).

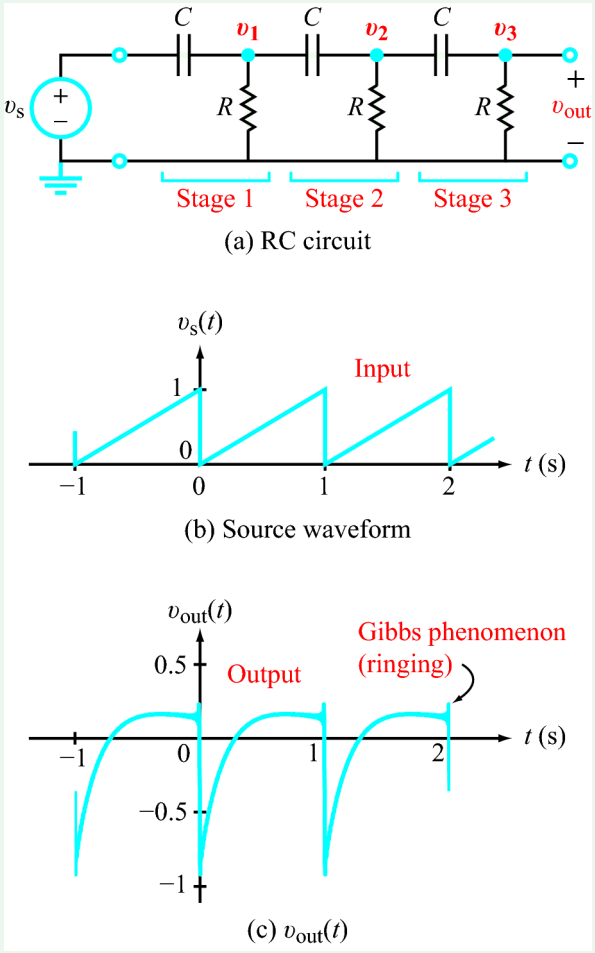


Figure 13.9 Circuit and plots for Example 13-6.

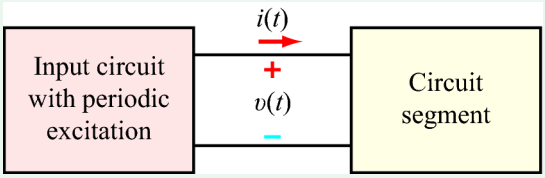


Figure 13.10 Voltage across and current into a circuit segment.

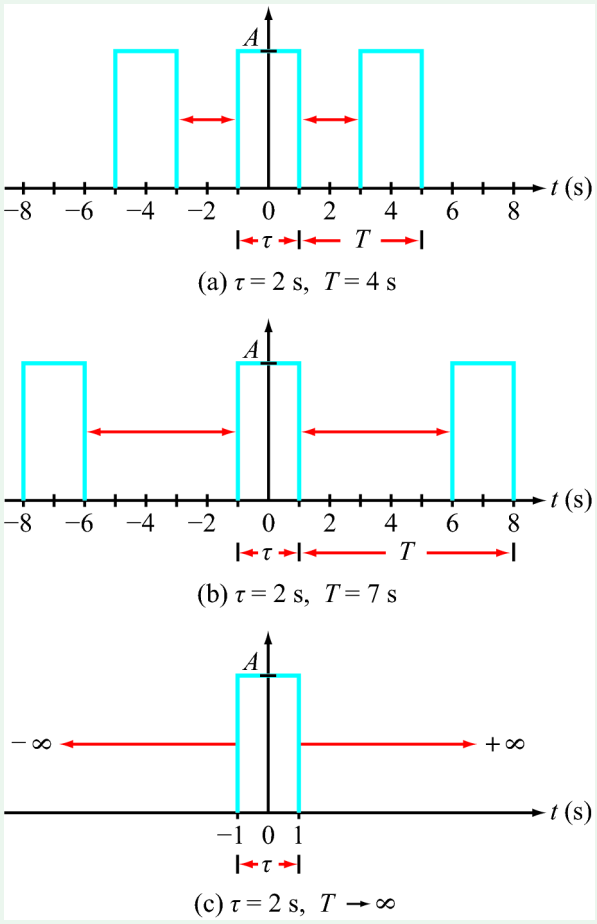


Figure 13.11 The single pulse in (c) is equivalent to a periodic pulse train with $T = \infty$.

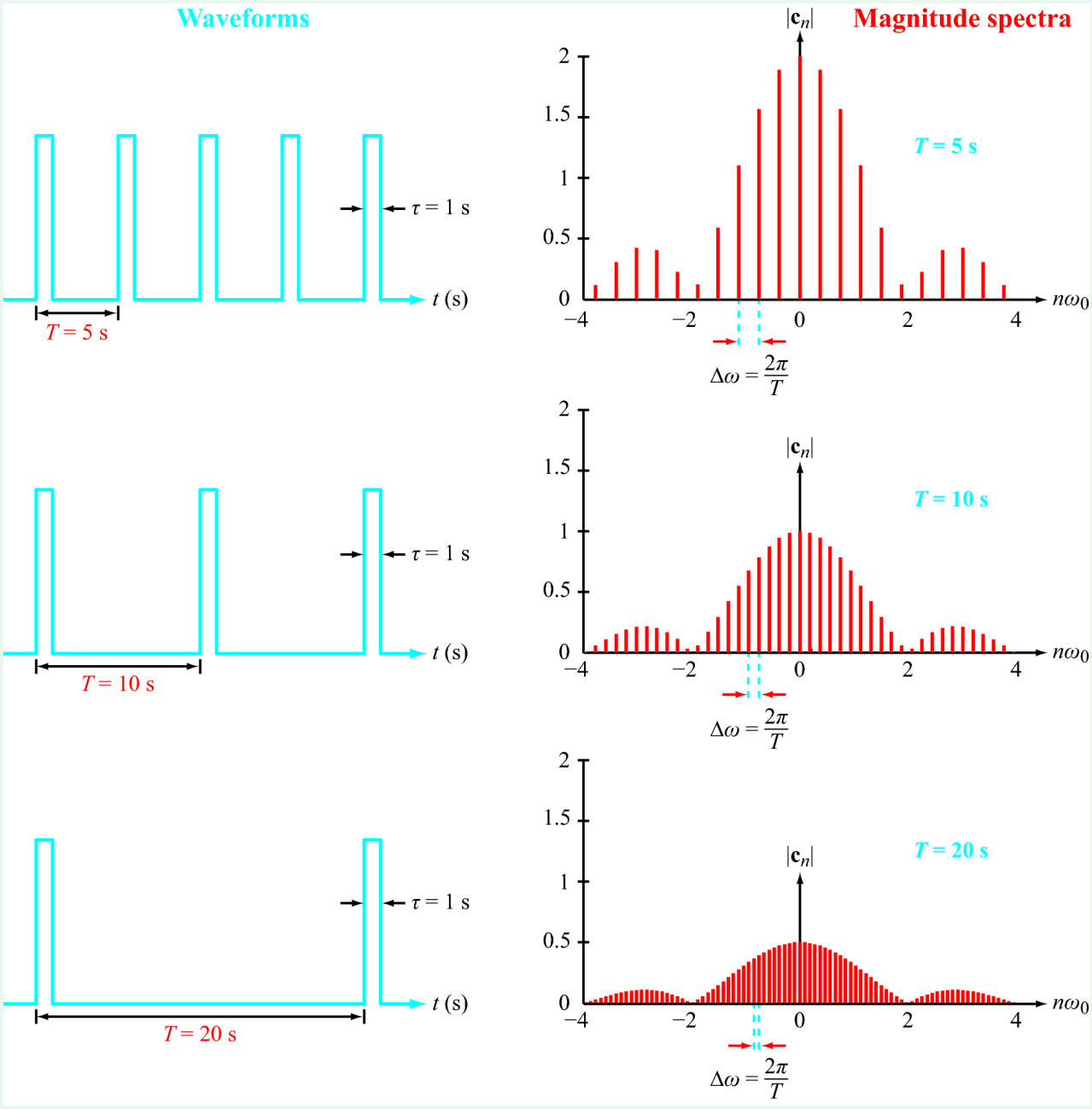


Figure 13.12 Line spectra for pulse trains with $T/\tau = 5$, 10, and 20.

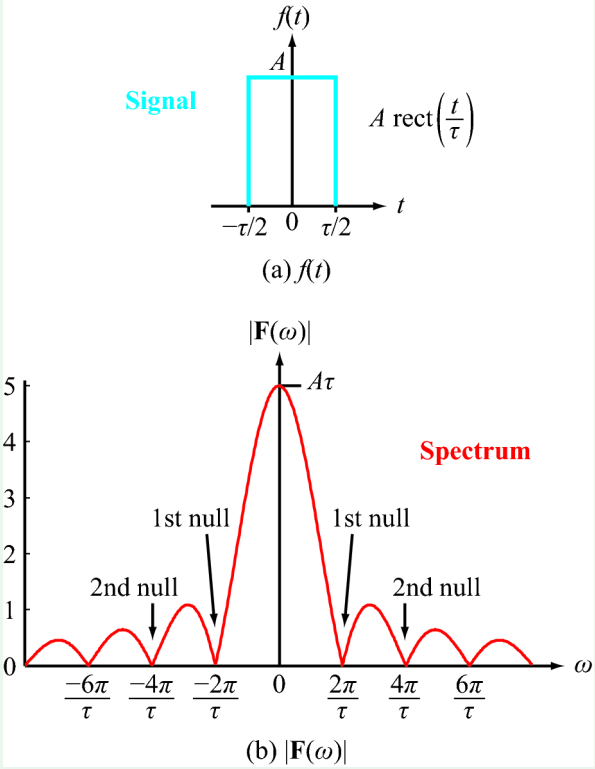


Figure 13.13 (a) Rectangular pulse of amplitude A and width τ; (b) frequency spectrum of $|\mathbf{F}(\omega)|$ for $A = 5$ and $\tau = 1$ s.

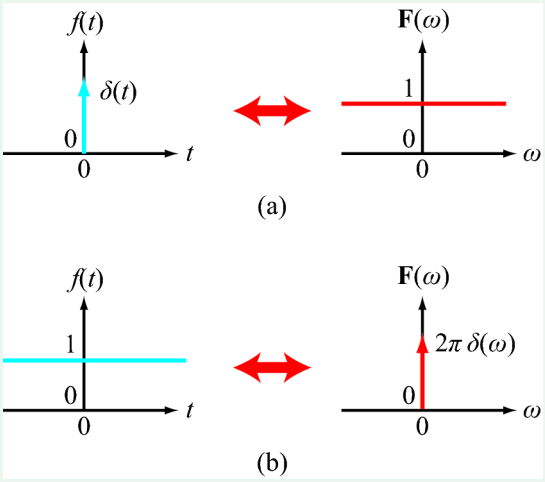


Figure 13.14 (a) The Fourier transform of $\delta(t)$ is 1 and (b) the Fourier transform of 1 is $2\pi\ \delta(\omega)$.

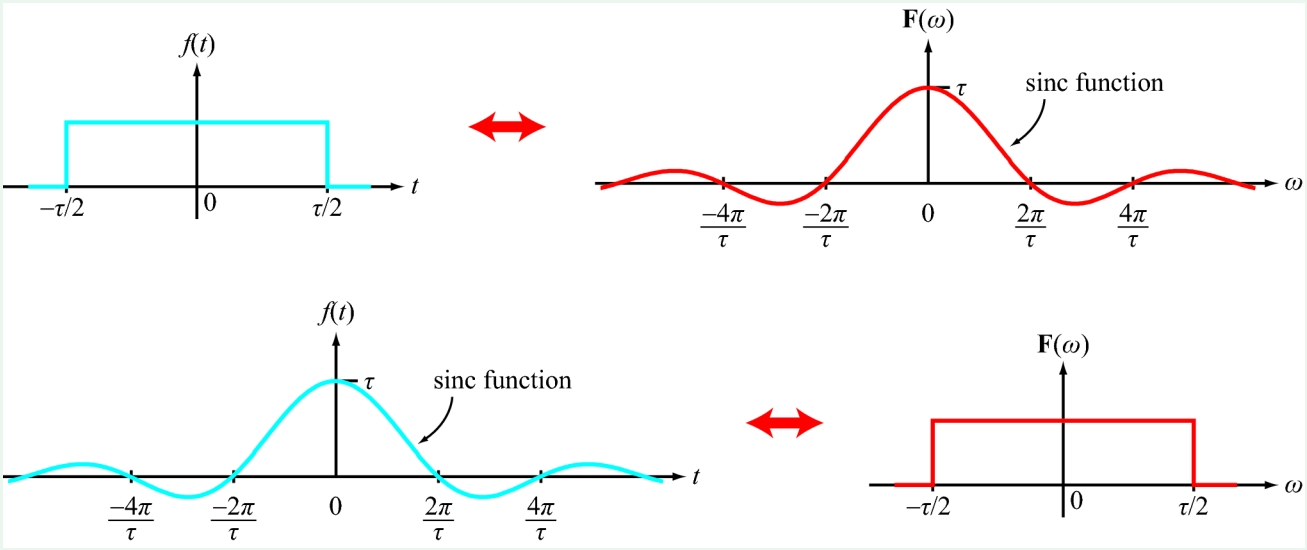


Figure 13.15 Time-frequency duality: a rectangular pulse generates a sinc spectrum and, conversely, a sinc-pulse generates a rectangular spectrum.

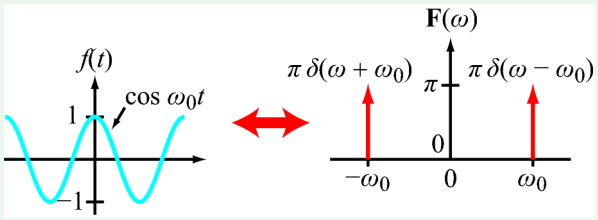


Figure 13.16 The Fourier transform of $\cos \omega_0 t$ is equal to two impulse functions—one at ω_0 and another at $-\omega_0$.

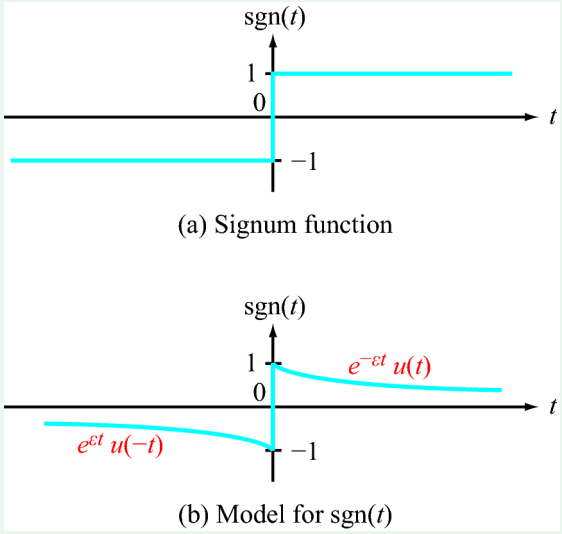


Figure 13.17 The model shown in (b) approaches the exact definition of $\text{sgn}(t)$ as $\varepsilon \to 0$.

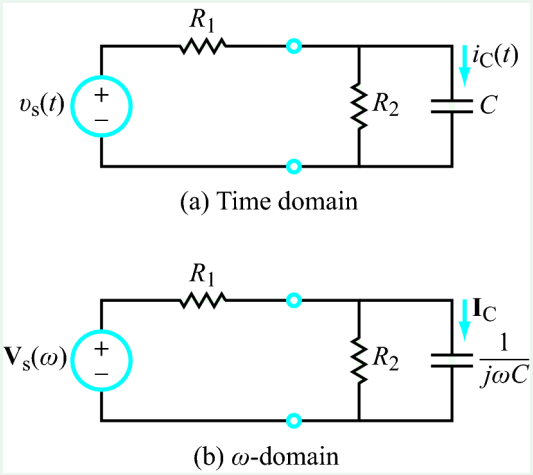


Figure 13.18 Circuits for Example 13-11.

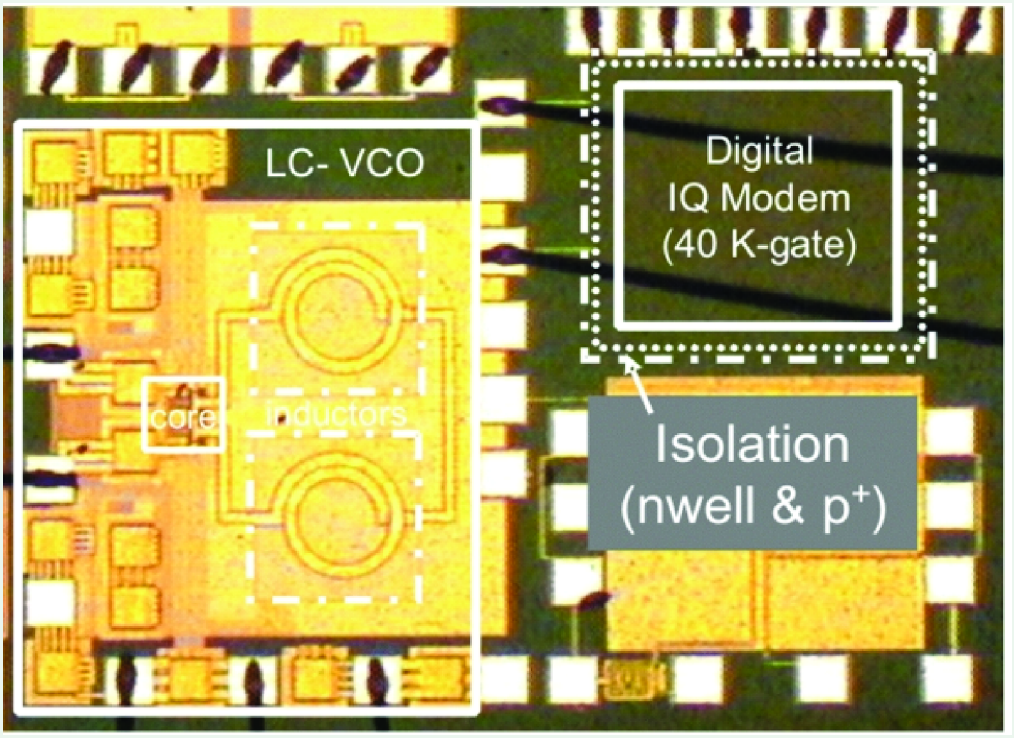


Figure 13.19 This mixed-signal chip implements a highly reconfigurable RF receiver based on a down-converting Sigma-Delta A/D (courtesy Renaldi Winoto and Prof. Borivoje Nikolic, U.C. Berkeley)

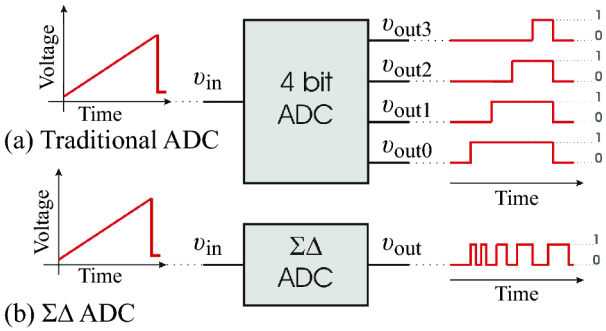


Figure 13.20 (a) A traditional 4-bit ADC converts an analog input voltage and produces 4 digital output bits; (b) a ΣΔ ADC generates a pulse train where the pulse duration is governed by the magnitude of the input voltage.

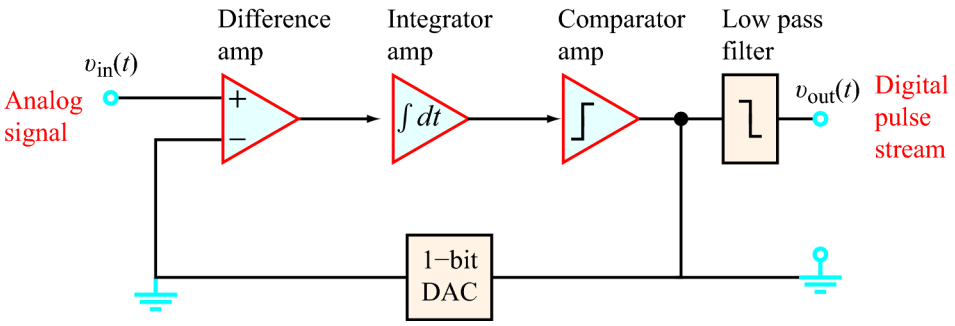


Figure 13.21 Block diagram of a ΣΔ modulator.

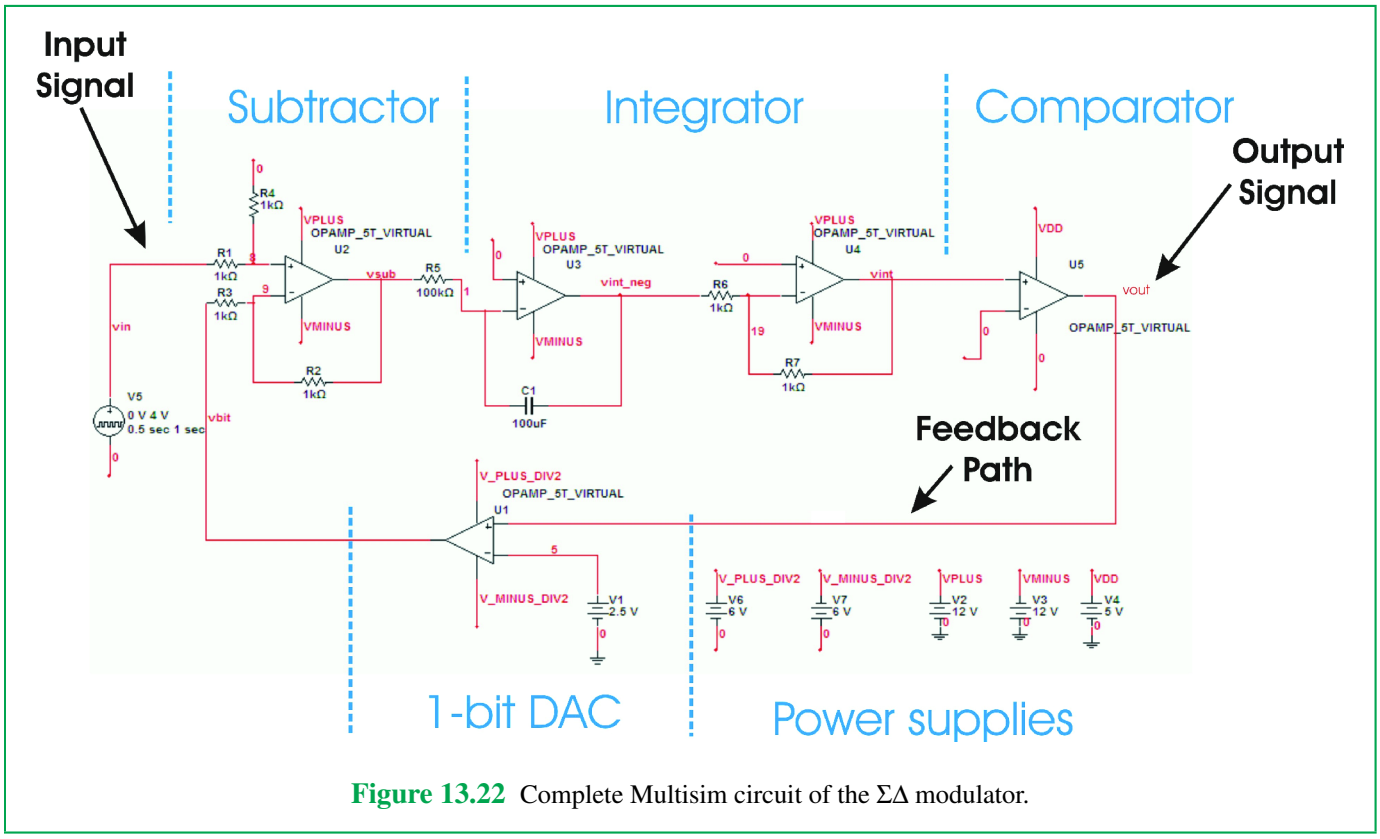


Figure 13.22 Complete Multisim circuit of the ΣΔ modulator.

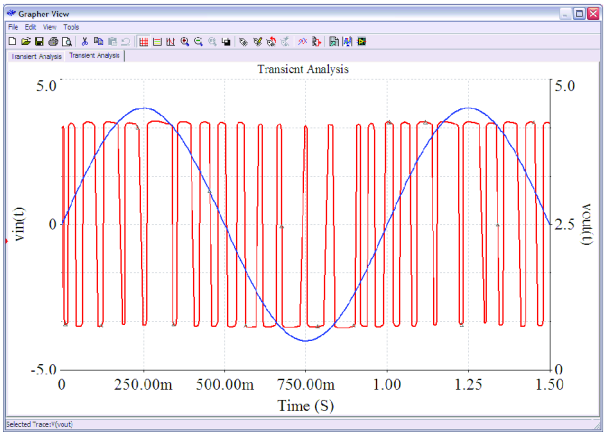


Figure 13.23 A 1 Hz sinusoidal ac signal, $\upsilon_{\text{in}}(t)$, blue trace, is converted to a series of pulses at the output, $\upsilon_{\text{out}}(t)$, red trace, by the Sigma Delta modulator. Note that the duration of the pulses is related to the instantaneous level of voltage $\upsilon_{\text{in}}(t)$.

